(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 361 614 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
07.11.2012 Bulletin 2012/45

(21) Application number: **02711222.6**

(22) Date of filing: **24.01.2002**

(51) Int Cl.:
H01L 21/04 *(2006.01)* ***H01L 29/78*** *(2006.01)*
H01L 21/316 *(2006.01)*

(86) International application number:
PCT/JP2002/000512

(87) International publication number:
WO 2002/059980 (01.08.2002 Gazette 2002/31)

(54) **SEMICONDUCTOR DEVICE MANUFACTURING METHOD**

HALBLEITERBAUELEMENTEHERSTELLUNGSVERFAHREN

PROCEDE DE FABRICATION D'UN DISPOSITIF SEMI-CONDUCTEUR

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

(30) Priority: **25.01.2001 JP 2001017680**

(43) Date of publication of application:
12.11.2003 Bulletin 2003/46

(73) Proprietors:
- **National Institute of Advanced Industrial Science and Technology**
  Tokyo 100-0013 (JP)
- **Japan Science and Technology Agency**
  Kawaguchi-shi
  Saitama 332-0012 (JP)
- **SANYO ELECTRIC CO., LTD.**
  Moriguchi-shi, Osaka-fu 570-8677 (JP)

(72) Inventors:
- **FUKUDA, Kenji,**
  Nat. Inst. of Advenced Ind. Science
  Tsukuba-shi,
  Ibaraki 305-8568 (JP)
- **ARAI, Kazuo,**
  Nat. Inst. of Advenced Ind. Science
  Tsukuba-shi,
  Ibaraki 305-8568 (JP)
- **SENZAKI, Junji,**
  Nat.Inst. of Advenced Ind. Science
  Tsukuba-shi,
  Ibaraki 305-8568 (JP)
- **HARADA, Shinsuke,**
  National Inst. of Advenced Ind.
  Tsukuba-shi,
  Ibaraki 305-8568 (JP)
- **KOSUGI, Ryoji,**
  Nat. Inst. of Advenced Ind. Science
  Tsukuba-shi,
  Ibaraki 305-8568 (JP)
- **ADACHI, K.,**
  Nat. Inst. of Advenced Ind. Science
  Tsukuba-shi,
  Ibaraki 305-8568 (JP)
- **SUZUKI, Seiji,**
  c/o Sanyo Electric Co., Ltd.
  Moriguchi-shi,
  Osaka 570-8677 (JP)

(74) Representative: **Faulkner, Thomas John et al**
Cleveland
10 Fetter Lane
London EC4A 1BR (GB)

(56) References cited:
WO-A-97/17730 **JP-A- 8 186 179**
JP-A- 8 186 179 **US-A- 5 151 759**
US-A- 6 028 012

- **LORI A LIPKIN ET AL: "Insulator Investigation on SiC for Improved Reliability" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 46, no. 3, March 1999 (1999-03), XP011016818 ISSN: 0018-9383**
- **ULRICH SCHMID ET AL: "High Temperature Performance of NMOS Integrated Inverters and Ring Oscillators in 6H-SiC" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE SERVICE CENTER, PISACATAWAY, NJ, US, vol. 47, no. 4, April 2000 (2000-04), XP011017219 ISSN: 0018-9383**

EP 1 361 614 B1

(Cont. next page)

- WANG X W ET AL: "High temperature (450/spl deg/C) reliable NMISFET's on p-type 6H-SiC" ELECTRON DEVICES MEETING, 1999. IEDM TECHNICAL DIGEST. INTERNATIONAL WASHINGTON, DC, USA 5-8 DEC. 1999, PISCATAWAY, NJ, USA,IEEE, US, 5 December 1999 (1999-12-05), pages 209-212, XP010372129 ISBN: 0-7803-5410-9
- PROVERBIO E ET AL: "Low-Temperature Oxidation of Silicon Nitride by Water in Supercritical Condition" JOURNAL OF THE EUROPEAN CERAMIC SOCIETY, ELSEVIER SCIENCE PUBLISHERS, BARKING, ESSEX, GB, vol. 16, no. 10, 1996, pages 1121-1126, XP004047418 ISSN: 0955-2219
- OPILA E J: "Variation of the Oxidation Rate of Silicon Carbide with Water-Vapor Pressure" JOURNAL OF THE AMERICAN CERAMIC SOCIETY, vol. 82, no. 3, 1999, pages 625-636, XP002472515
- WILLIAM E. WAGNER ET AL.: 'Characterization of silicon carbid e(SiC) epitaxial channel MOSFETs' IEEE TRANSACTIONS ON ELECTRON DEVICES vol. 47, no. 11, November 2000, pages 2214 - 2220, XP000970490
- LORI A. LIPKIN ET AL.: 'Insulator investigation on SiC for improved reliability' IEEE TRANSACTIONS ON ELECTRON DEVICES vol. 46, no. 3, March 1999, pages 525 - 532, XP000926942
- MAN PIO LAM ET AL.: 'Punchthrough behavior in short channel NMOS and PMOS 6H-silicon carbide transistors at elevated temperatures' IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGY vol. 22, no. 3, September 1999, pages 433 - 438, XP002951595
- LORI A. LIPKIN ET AL.: 'SiC devices with ONO stacked dielelectrics' MATERIALS SCIENCE FORUM-1999 vol. 338-342, 2000, pages 1093 - 1096, XP002951596
- KATSUNORI UENO ET AL.: 'Counter-doped MOSFET's of 4H-SiC' IEEE ELECTRON DEVICE LETTERS vol. 20, no. 12, December 1999, pages 624 - 626, XP000890738
- ULRICH SCHMID ET AL.: 'High temperature performance of NMOS integrated inverters and ring oscillators in 6H-SiC' IEEE TRANSACTIONS ON ELECTRON DEVICES vol. 47, no. 4, April 2000, pages 687 - 691, XP000947260
- SCOTT T. SHEPPARD ET AL.: 'Characteristics of inversion-channel and buried-channel MOS devices in 6H-SiC' IEEE TRANSACTIONS ON ELECTRON DEVICES vol. 41, no. 7, July 1994, pages 1257 - 1264, XP000453328

Description

Technical Field:

[0001] This invention relates to a method of manufacturing a metal-insulator-semiconductor (MIS) field-effect transistor that is fabricated on a silicon carbide substrate in which the crystal surface orientation of the substrate is prescribed and the impurity diffusion layer is optimized, particularly to a method of manufacturing a semiconductor device in which the method of forming a gate insulation layer and the following heat treatment are contrived.

Background Art:

[0002] A number of inventions have already been disclosed relating to a method of oxidizing a silicon carbide substrate and the following heat treatment method, and to an MIS field-effect transistor having a buried channel region.

[0003] For example, U.S. Patent No. 5,864,157 describes a structure that, in a flash memory having dual gates, uses a P-type electrode for the lower gate and an N-type impurity for the buried channel region. However, this description relates to a flash memory having dual gates, which is different from the structure of the present invention. Also, there is no description concerning the concentration of the P-type polysilicon electrode and the impurity concentration of the buried channel region, and the relationship between the depth of the source region or drain region and the depth of the channel region.

[0004] In JP-A HEI 8-186179, there is described a structure, in an N-channel transistor having an LDD structure, that uses a P-type electrode for the gate electrode and an N-type impurity for the buried channel region. However, in this JP-A HEI 8-186179, there is no description concerning the impurity concentration of the P-type polysilicon electrode and the relationship between the depth of the source region or drain region and the depth of the channel region.

[0005] Also, JP-A HEI 7-131016 describes an MIS field-effect transistor structure characterized by the transistor channel formation surface being parallel to the (1, 1, -2, 0) surface of the hexagonal silicon carbide single-crystal substrate. However, this JP-A HEI 7-131016 does not describe anything relating to a buried channel region type MIS field-effect transistor that uses a P-type electrode for the gate electrode.

[0006] With respect to a method of oxidizing a silicon-carbide substrate, U.S. Patent No. 5,972,801 describes a method that, following formation of the gate oxide layer, includes exposing the gate oxide layer to an atmosphere containing water vapor at a temperature of 600°C to 1000°C, but this process is carried out under conditions whereby there is no increase in the thickness of the gate oxide layer of the silicon carbide substrate that is thus further oxidized. This differs from the present invention, in that in the present invention, the silicon carbide substrate is slightly oxidized and the thickness of the gate oxide layer is increased.

[0007] JP-A HEI 5-129596 discloses a process for dry oxidation and wet oxidation of a silicon substrate. From the description, this is a process that increases the gate layer thickness by using wet oxidation to oxidize a semiconductor substrate, as understood from the description, "(A) is when dry oxidation is performed for 85 minutes, making the thickness of the gate oxide layer 25.3 nm, and (B) is when, similarly, dry oxidation is performed for 80 minutes, after which wet oxidation is performed for 1 minute, making the thickness of the gate oxide layer 26.3 nm."

[0008] However, this JP-A HEI 5-129596 shows no disclosure relating to the composition of a buried channel type MIS field-effect transistor. It is known that in this type of transistor, the performance is highly dependent on the profile of the diffused impurity. Therefore, the relationship between the heat treatment in the oxidizing process and the introduction of the impurity is important. With respect to the impurity that is introduced, because the present invention uses a silicon carbide substrate having a diffusion coefficient that is lower than that of a silicon substrate, it is possible to use heat treatment for the purpose of oxidation, after forming the diffusion layer used for the buried channel, and the source/drain diffusion layer. The present invention differs from the invention of the JP-A HEI 5-129596 in that it discloses a process that allows the use of a silicon carbide substrate.

[0009] High Temperature Performance of NMOS Integrated Inverters and Ring Oscillators in 6H-SiC-IEEE Transactions on Electron Devices, vol. 47, n.4, April 2000, describes the fabrication of a SiC this transitor having a polysilicon gate.

[0010] US 5 151 759 shows a silicon-on-insulator field-effect transistor. The channel region is formed after the formation of a standard oxide layer by implanting low energy ions through the oxide layer.

[0011] Insulator Investigation on SiC for Improved Reliability - IEEE Transactions on Electronic Devices, Vol.46 no. 3, March 1999, pages 525-532, describes various production methods for SiC metal-insulator-semiconductor devices including dry-wet oxidation processes.

Disclosure of the Invention:

[0012] Compared to a silicon MIS transistor, the interfacial level density of an oxide layer-silicon oxide interface using a silicon carbide substrate generally is approximately one order of magnitude higher. Therefore, an MIS field-effect

transistor that uses a silicon carbide substrate has a problem that channel mobility is approximately one order of magnitude lower than that of an MIS field-effect transistor that uses a silicon substrate. In the case of a silicon MIS transistor, it is known that a buried channel region type MIS field-effect transistor is superior because the flow of electrons from the source to the drain is not readily affected by the above interface between oxide layer and silicon carbide. But, when a silicon MIS transistor on a silicon carbide substrate is made as a buried channel region type structure that is not optimized, it readily becomes normally on (a phenomenon where current flows between source and drain even when the gate voltage is zero). Also, in cases where optimization is not attempted, hot carrier resistance is poor and adequate punch-through resistance cannot be achieved.

[0013] This invention was proposed in consideration of the above and, in a semiconductor device using a silicon carbide substrate, it would be desirable to provide a method of manufacturing a semiconductor device that is a buried channel region type transistor that by optimizing the structure of the burned channel region type MIS transistor, gate insulation layer formation method and surface orientation of the silicon carbide substrate, does not become normally on and, moreover, has high hot-carrier resistance, high punch-through resistance and high channel mobility.

[0014] The present invention relates to a method of manufacturing an MIS field-effect transistor as claimed in claim 1.

[0015] The gate electrode may include a high-melting-point metal silicide layer.

[0016] The high-melting-point metal silicide layer may be a tungsten, molybdenum or titanium silicide layer.

[0017] In a development that relates to a hot-carrier resistance improvement technology the semiconductor device has a region between a region in which the buried channel region is formed and the source or drain region having an impurity concentration that is not lower than a maximum impurity concentration of an impurity diffusion layer region used to form the buried channel region, and not higher than an impurity concentration of the source or drain region.

[0018] The region between a region in which the buried channel is formed and the source or drain region, may include a diffusion layer of nitrogen, phosphorus or arsenic at a maximum concentration that is 5 x 10^{10}cm^{-3} to 5 x 10^{19}cm^{-3}.

[0019] In a development that relates to punch-through resistance improvement.

[0020] Located adjacently beneath the region in which the buried channel is formed, there is a P-type impurity diffusion region having an impurity concentration that is higher than an impurity concentration of the semiconductor substrate.

[0021] The semiconductor device may-have a high-concentration P-type impurity diffusion region located adjacently beneath the region in which the buried channel is formed that includes an aluminum or boron diffusion layer having a maximum impurity concentration of 1 x 10^{17} cm^{-3} to 1 x 10^{19}cm^{-3}.

Brief Description of Drawings:

[0022]

Figure 1 is a diagram showing stages in a preferred process for manufacturing an MIS field-effect transistor having a P-type gate electrode and a buried channel region.

Figure 2 is a diagram showing the relationship between channel mobility and threshold voltage in an MIS field-effect transistor with a gate electrode of P-type polycrystalline silicon, N-type polycrystalline silicon, and aluminum, in which L_{bc} = 0.3 gm, Xj = 0.5 μm, the impurity concentration of the buried channel region is 2 x 10^{16} cm^{-3}, and the impurity concentration of the P-type polycrystalline silicon is 5 x 10^{20} cm^{-3}.

Figure 3 is a diagram showing the L_{bc} ÷ Xj dependency of the channel mobility of a buried channel in a P-type polycrystalline silicon gate electrode, in which the impurity concentration is 5 x 10^{20} cm^{-3}, L_{bc} = 0.3 μm, Xj = 0.5 μm, and the impurity concentration of the buried channel region is 2 x 10^{16}cm^{-3}.

Figure 4 is a diagram showing the relationship between the impurity concentration of the P-type polycrystalline silicon gate and the threshold voltage, in which L_{bc} = 0.3 μm, Xj = 0.5 μm, and the impurity concentration of the P-type polycrystalline silicon is 2 x 10^{16} cm^{-3}.

Figure 5 is a diagram showing the relationship between channel mobility and the impurity concentration of the buried channel region, in which L_{bc} = 0.3 μm, Xj = 0.5 μm, and the impurity concentration of the P-type polycrystalline silicon is 5 x 10^{20} cm^{-3}.

Best Mode for Carrying out the Invention:

[0023] In the following, details of the modes of this invention are described with reference to the following examples.

Example 1:

[0024] First, as an example of a preferred manufacturing process of this invention, Example 1 is shown in Figures 1 (a), 1(b) and 1(c), and will be explained in order, with the experiments conducted to obtain the data of Figure 2 through Figure 5.

[0025] After a P-type silicon carbide substrate 1 (4H-SiC, impurity concentration: 5 x 10^{15} cm^{-3}) shown in Figure 1(a) has been subjected to ordinary RCA cleaning, RIE (reactive ion etching) is used to form photolithography alignment marks on the P-type silicon carbide substrate 1. Next, in order to investigate the punch-through resistance improvement effect, a number of samples were prepared by using aluminum ion implantation to form a punch-through prevention region 3 at a depth that placed the region just below a buried channel region; the punch-through prevention region 3 was given a higher impurity concentration of 1 x 10^{16} cm^{-3} to 1 x 10^{19} cm^{-3} than that of the P-type silicon carbide substrate 1.

[0026] Next, ion implantation of an N-type impurity, such as nitrogen, phosphorus or arsenic, is used to form the buried channel region 2. If phosphorus, for example, is used to form a buried channel region at a junction depth (L_{bc}) of 0.3 μm, the desired profile is formed using multiple implantations at 40 to 250 keV to provide a total dose to achieve a concentration of 7 x 10^{15} cm^{-3}. With the manufacturing process shown in this example, to investigate the relationship between the ratio between L_{bc} and the depth (Xj) of a source 5 and drain 6 shown in Figure 1(b), and the channel mobility, a buried channel region 2 was formed at a depth (L_{bc}) of 0.1, 0.2, 0.3, 0.4 and 0.5 μm. To investigate the concentration dependency of the buried channel region 2 with respect to channel mobility, ion implantation was used to prepare samples having concentrations of 5 x 10^{15} cm^{-3} to 5 x 10^{17} cm^{-3} at an L_{bc} of 0.3 μm.

[0027] Next, thermal oxidation or CVD (chemical vapor deposition) is used to form a SiO_2 layer for an ion implantation mask 4 for the source region and drain region, as shown in Figure 1(b). In this example, as shown in Figure 1(b), an LTO (low-temperature oxide) layer is used for the implantation mask. By reacting silane and oxygen at 400°C to 800°C to form silicon dioxide deposited on the P-type silicon carbide substrate 1, thereby forming the LTO layer. Then, after using lithography to form the source and drain regions, HF (hydrofluoric acid) is used to etch the LTO and expose the ion implantation source and drain regions. Next, to form the source 5 and drain 6 shown in Figure 1(b), ion implantation at 500°C is used to implant nitrogen, phosphorus or arsenic at a depth (Xj) of 0.5 μm. In this example, as in the case of the formation of the buried channel region 2, multiple implantation steps are used to form a phosphorus concentration of 5 x 10^{19} cm^{-3}.

[0028] This is followed by activation annealing for 30 minutes at 1500°C in an argon atmosphere. This is followed by oxidation at 1200°C for approximately 150 minutes in a gas containing O_2 or for approximately 90 minutes in a gas containing water vapor, to form a gate insulation layer 7 approximately 50 nm thick. The following methods are known for oxidation using a gas containing water vapor.

1) Using oxygen or inert gas (argon, nitrogen or helium) to flow water vapor heated to steam up to the silicon carbide substrate.
2) Combusting H_2 and O_2 at 900°C to generate steam that is flowed up to the silicon carbide substrate. In this case too, water vapor can be flowed together with inert gas.

[0029] While either method can be used, here method 2) is used. Next, after being annealed for 30 minutes in an argon atmosphere, the samples were cooled in argon to room temperature. This step can be omitted. Also, to investigate the effect of the heat treatment in an atmosphere containing water vapor, some of the samples were heat-treated at 950°C for 3 hours by combusting H_2 and O_2 at 800°C to generate steam that was flowed up to the silicon carbide substrate. Here too, water vapor can be flowed together with inert gas.

[0030] After that, a P-type gate electrode 8 is formed. There are a number of methods for doing this, as shown below.

1) P-type polycrystalline silicon is formed using the CVD method to form polycrystalline silicon, followed by boron or boron fluoride ion implantation.
2) P-type polycrystalline silicon is formed using the CVD method to form polycrystalline silicon, followed by the formation of a boron-containing SiO_2 film by the CVD method or by spin-coating, and using heat treatment at 800°C to 1100°C to effect diffusion.
3) P-type polycrystalline silicon is formed flowing silane and diborane together and heat-treating at 600°C to grow the polycrystalline silicon while diffusing boron.

[0031] In this example, method 2) is used. Here, the diffusion time was changed at 900°C to form P-type polycrystalline silicon with an impurity concentration of 1 x 10^{15} cm^{-3} to 1 x 10^{21} cm^{-3}, and the relationship between the impurity concentration of the P-type gate electrode and the channel mobility was investigated. To investigate the effect of the silicide film, using a number of samples, high-melting-point metal silicide layers 9 of WSi_2, $MoSi_2$ and $TiSi_2$ were formed on the P-type polycrystalline silicon. The P-type polycrystalline silicon or the composite silicide and P-type polycrystalline silicon layer and the gate insulation layer were then etched to form the gate electrode. Following this, the oxide film over the source and drain regions was then etched to form contact holes. Then, vapor deposition or sputtering was used to form a metal-containing layer or laminated layer of nickel, titanium or aluminum, and RIE or wet etching was used to form metal wires 10. In this example, vapor deposition of nickel was used, followed by wet etching. To ensure good ohmic contact, the samples were then heat-treated for 5 minutes at 1000°C in an argon atmosphere, thereby completing

the MIS field-effect transistors.

[0032] Table 1 shows a comparison of the effect of the gate oxidation method, post-oxidation heat treatment and buried channel structure on the channel mobility of a MOSFET according to the above process.

Table 1

	Ordinary MOSFET		Buried channel MOSFET	
Gate oxidation method	Argon treatment	Treatment after water vapor	Argon treatment	Treatment after water vapor
Dry oxidation	10 cm^2/Vs	25 cm^2/Vs	Normally on	140 cm^2/Vs
Wet oxidation	10 cm^2/Vs	15 cm^2/Vs	50 cm^2/Vs	125 cm^2/Vs

[0033] In each case, the process shown was under the following conditions.

1) Dry oxidation: Oxidizing for 150 minutes at 1200°C using only oxygen containing no water vapor.
2) Wet oxidation: Combusting H_2 and O_2 at 900°C to generate water vapor that is flowed up to the substrate, oxidizing for 90 minutes at 1200°C.
3) Argon treatment: Following formation of oxide film, 30 minutes of heat treatment at 1200°C in argon, and cooling treatment.
4) Treatment after water vapor: Following argon treatment, combusting H_2 and O_2 at 800°C to generate water vapor that is flowed up to the silicon carbide substrate, heat-treating for 3 hours at 950°C, then cooling to room temperature.

[0034] From Table 1, it can be understood that in the case of an ordinary MOSFET, by just using argon heat treatment after forming the gate insulation layer, channel mobility is the same with respect to both dry oxidation and wet oxidation (both being 10 cm^2/Vs), but when heat treatment in a water vapor atmosphere is also used, channel mobility is 25 cm^2/Vs in the case of dry oxidation and 15 cm^2/Vs in the case of wet oxidation, so channel mobility is improved by using water vapor treatment after gate layer formation.

[0035] Moreover, channel mobility is higher when dry oxidation is used to form the gate oxidation layer. This is the same in the case of a buried channel structure MOSFET. Gate oxidation by dry oxidation using just argon heat treatment resulted in a normally on condition, making the device unusable in practice, but forming the gate insulation layer by water vapor oxidation resulted in a channel mobility that, at 50 cm^2/Vs, was improved by the buried channel structure.

[0036] Furthermore, when water vapor treatment is used after gate insulation layer formation, in the case of gate insulation layer formation by dry oxidation channel mobility is 140 cm^2/Vs and 125 cm^2/Vs in the case of water vapor oxidation, showing that a combination of buried channel structure and post-oxidation water vapor treatment produces a major improvement in channel mobility. In particular, channel mobility became highest when the gate insulation layer was formed using dry oxidation.

[0037] Using water vapor treatment after gate insulation layer formation increased the thickness of the gate insulation layer very slightly (by around 0.1 to 0.5 nm), but in calculating the channel mobility, it was assumed that there was no change in the gate insulation layer thickness. Therefore, in practice, it can be understood that the difference in channel mobility is very slightly larger than the above values.

[0038] Viewing the time of the water vapor treatment following gate insulation layer formation as a function, channel mobility improves as the water vapor treatment time is increased from 0 (zero). However, when water vapor treatment was carried out over an extended time, channel mobility showed a tendency to decrease. Therefore, the above water vapor treatment is effective up to a time (critical time) at which channel mobility is exhibited that is below the channel mobility when water vapor treatment is not used. However, because this critical time varies depending on substrate impurity concentration and the like, it cannot be uniformly specified. Also, it can be readily understood that there is an optimum time at which maximum channel mobility is reached. It is desirable for the time of the water vapor treatment of the present invention to be carried out in this optimum time.

[0039] Figure 2 shows the measurement-based relationship between channel mobility and threshold voltage in a MIS field-effect transistor with a gate electrode using P-type polycrystalline silicon, N-type polycrystalline silicon and aluminum. Compared using the same threshold voltage, channel mobility is higher with a gate electrode that uses P-type polycrystalline silicon than that of a gate electrode that uses N-type polycrystalline silicon or aluminum. This is due to the fact that, depending on the gate electrode polarity, a different amount of ion implantation is required to achieve the same threshold voltage; possible reasons are detailed below.

[0040] Implantation of N-type impurity into the buried channel region 2 results in the center of the channel being formed at a deep location away from the interface between the gate insulation layer and the P-type silicon carbide substrate 1.

Since this increases the number of carriers that are not readily susceptible to the effect of the high field near the interface, channel mobility is increased. Mobility is also increased by a low channel concentration of implanted P-type impurity. However, if the N-type impurity in the buried channel region 2 is increased to increase the channel mobility, the threshold voltage decreases, becoming a negative voltage, creating a state in which current flows even at a zero voltage, that is, a normally on state.

[0041] It is known that, in general, the threshold voltage of the MIS field-effect transistor becomes larger as the work function differential between a gate electrode and a semiconductor becomes larger. With reference to the work function differential between the gate electrode and the semiconductor, it is also known that there is almost no change when aluminum or N-type polycrystalline silicon is used for the gate electrode, but when P-type polycrystalline silicon is used, compared to the semiconductor substrate, it becomes approximately one volt more. Therefore, even when N-type impurity is implanted in the channel region, the tendency for the threshold voltage to go negative and create a normally on state can be suppressed by using P-type polycrystalline silicon for the gate electrode, so that even with the same threshold voltage, channel mobility can be increased by implanting an impurity concentration for forming the buried channel region that is higher compared to aluminum and N-type polycrystalline silicon used for the gate electrode. This makes it possible to form a channel at a deeper location, therefore making it possible to increase the channel mobility.

[0042] Figure 3 is a graph showing the $L_{bc} \div Xj$ dependency of the channel mobility, when the junction depth Xj of the source and drain diffusion layers is 0.5 μm. In Figure 3, the vertical axis shows the normalized channel mobility of a sample having no buried channel region. The evaluation was performed using an L_{bc} of 0.2 or more; it was confirmed that there was an effect even at 0.2. Therefore, the lower limit on the horizontal axis was set at 0.2. At over 1 on the horizontal axis, channel mobility increases, but the threshold voltage goes negative, resulting in a normally on state that makes the device difficult to use in practice. Therefore, the horizontal axis is limited to 0.2 to 1.0. A range of 0.4 to 1.0 is particularly effective.

[0043] Figure 4 shows the measured relationship between the impurity concentration of the P-type polycrystalline silicon gate and the threshold voltage. A higher concentration increases the work function differential between the gate electrode and the semiconductor substrate, increasing the threshold voltage. Conversely, a lower concentration decreases the threshold voltage, which at 1×10^{16} cm^{-3} becomes zero. Therefore the lower limit for the impurity concentration is set at 1×10^{16} cm^{-3}, and since the concentration of boron capable of being implanted into polycrystalline silicon is 1×10^{21} cm^{-3}, the upper limit is set at 1×10^{21} cm^{-3}.

[0044] Figure 5 shows the measured relationship between channel mobility (using the value at an impurity concentration of zero as the standard value) and the impurity concentration of the buried channel region 2. The lower limit of the evaluation impurity concentration was $5 \times 10^{16} cm^{-3}$. Since an adequate effect was achieved with that value, the lower limit was set at 5×10^{15} cm^{-3}. With a concentration of 1×10^{18} cm^{-3} or more, the threshold voltage goes negative, making the device hard to use, so the upper limit was set at 1×10^{18} cm^{-3}.

[0045] If the impurity concentration of the P+ punch-through prevention region provided under the buried channel region 2 to suppress punch-through is lower than 1×10^{17} cm^{-3}, the gate voltage that gives rise to punch-through is the same as when there is no P+ region, which is the same as no effect. A concentration of at least 1×10^{17} cm^{-3} increases the gate voltage at which punch-through occurs, so the lower limit is 1×10^{17} cm^{-3}. If the impurity concentration is 1×10^{19} cm^{-3} or higher, the impurity diffuses during activation annealing, offsetting the N-type impurity in the channel region above, making it impossible for the buried channel region to function as required. Therefore, the upper limit is 1×10^{19} cm^{-3}.

[0046] The specific resistance of polycrystalline silicon given a high boron concentration is on the milliΩcm level, but the specific resistances of the high-melting-point metal silicides, for example $MoSi_2$, WSi_2 and $TiSi_2$ are 60 μΩcm, 50 μΩcm and 15 μΩcm, respectively, so the specific resistance of a gate electrode that is a composite of polycrystalline silicon and silicide is lower compared to polycrystalline silicon in which impurity has been implanted. As such, it can be readily understood that even when P-type polysilicon is used, from the standpoint of configuring a circuit, it is more advantageous to use a polycide structure that is a laminated layer of polycrystalline silicon and silicide. When a polycide structure is thus used, the threshold value becomes substantially equal to what it is when only P-type polysilicon is used, so the channel mobility also becomes substantially the same in this case.

Example 2:

[0047] An example that differs from the above example will now be described as Example 2. Figures 1(a), 1(b) and 1(d) show the order of a specific manufacturing process of Example 2.

[0048] After a P-type silicon carbide substrate 1 (impurity concentration: 5×10^{15} cm^{-3}) shown in Figure 1(a) was subjected to ordinary RCA cleaning, RIE (reactive ion etching) was used to form photolithography alignment marks on the P-type silicon carbide substrate 1. Next, phosphorus ion implantation was used to form a buried channel region 2 at a junction depth L_{bc} of 0.3 μm, using multiple implantations at 500°C and 40 keV to 250 keV to provide a total dose for a concentration of 7×10^{15} cm^{-3}. Then, as shown in Figure 1(b), to form an ion implantation mask, an LTO layer was formed over the whole surface and photolithography was used to leave the gate electrode portion resist, with hydrofluoric

acid being used to etch the LTO layer. Then, to investigate the hot-carrier resistance effect of the impurity concentration between the buried channel region 2 and the source 5 or drain 6, ion implantation of phosphorus at 500°C was used to form a - low-impurity-concentration region 11 having an impurity concentration of 5×10^{16} cm^{-3} to 5×10^{20} cm^{-3} between the buried channel region 2 of Figure 1(d) and the source 5 or drain 6. Next, to form the source region 5 and drain region 6, an LTO layer was formed over the whole surface and photolithography used to form a photoresist to define the source and drain regions, and HF (hydrofluoric acid) was used to etch the LTO layer and expose the ion implantation source and drain regions. The source 5 and drain 6 were then formed using multiple ion implantations of phosphorus at 500°C to form an impurity concentration of 5×10^{19} cm^{-3}. This was followed by activation annealing for 30 minutes at 1500°C in an argon atmosphere.

[0049] For each sample, this was followed by dry oxidation at 1200°C for 150 minutes, forming a gate insulation layer 7 approximately 50 nm thick. After being annealed for 30 minutes in an argon atmosphere, the samples were cooled in argon to room temperature. Samples were also fabricated that were heat treated at 950°C for 3 hours in a water vapor atmosphere, annealed for 30 minutes in argon, then cooled to room temperature in argon. The P-type gate electrode 8 was then formed by using the CVD method to form polycrystalline silicon, and by using spin coating to form a boron-containing oxide film on the polycrystalline silicon followed by 30 minutes of heat treatment at 900°C to diffuse boron from the boron-containing oxide film to the polysilicon. The P-type polycrystalline silicon and the gate insulation layer were then etched to form the gate electrode. Next, LTO was deposited over the whole surface of the oxide layer and the oxide film over the source 5 and drain 6 was etched to form contact holes. The electron-beam deposition method was then used to form a nickel film over-the layer, and wet etching was used to form metal wires 10. To form a good ohmic contact, the samples were then heat-treated for 5 minutes at 1000°C in an argon atmosphere, thereby completing the MIS field-effect transistors.

[0050] The transistors were subjected to an electrical stress for a set time, and the degree by which the threshold voltage changed was measured to evaluate hot-carrier resistance. A smaller change in threshold voltage indicated good hot-carrier resistance. The threshold voltage was obtained as the voltage at which, with 0.1 volt applied to the drain and with the source at 0 volt, along a gate voltage of zero to 30 volts, the square of half the drain current intersects the plotted voltage axis. The electrical stress comprised applying 5 volts to the drain and 2.5 volts to the gate, for five minutes. The transistors measured were those in which ion implantation of phosphorus was used to form an impurity concentration of 5×10^{16} cm^{-3} to 5×10^{19} cm^{-3} between the buried channel region 2 and the source or drain region. A low impurity concentration in this region results in a larger depletion layer owing to which a field is smaller in the vicinity of the drain, making it possible to prevent electrons that pass through the region from entering a high-energy state, thereby improving hot-carrier resistance by decreasing the number of electrons that are implanted into the gate insulation layer from the substrate by scattering. However, if the impurity concentration of this region is too low, the resistance of the region will become too high, reducing the driving force of the transistor, leading to a lower limit of 5×10^{16} cm^{-3}. If the concentration is too high, the field in the vicinity of the drain will not be alleviated, making it impossible to attain sufficient hot-carrier resistance. From measurements, it was found that with a concentration of 5×10^{19} cm^{-3} or more, the amount of change in threshold voltage exceeded 10%. That much change is too much for practical use. Therefore, the upper limit became 5×10^{19} cm^{-3}.

[0051] While the foregoing description has been made with reference to the use of silicon carbide, it can be readily understood that the effect will be the same with a semiconductor substrate using diamond, silicon, gallium nitride or other such semiconductor.

Industrial Applicability:

[0052] Embodiments of this invention constituted as described in the foregoing have the applicability described below.

[0053] Methods of manufacturing a semiconductor device using a P-type gate electrode that includes heat treatment in an atmosphere containing water vapor, following gate insulation layer formation. This makes it possible to use a relatively high N^- concentration without the device becoming normally on, making it possible to increase channel mobility.

[0054] The ratio between the junction depth Xj of the source and drain regions and the junction depth L_{bc} of the buried channel region junction may be optimized, and after its formation the gate insulation layer is heat-treated in an atmosphere containing water vapor, which enables the channel mobility to be improved.

[0055] In addition to the above two steps, the concentration of the P-type polycrystalline silicon may be optimized, and after its formation the gate insulation layer may be heat-treated in an atmosphere containing water vapor, which enables the channel mobility to be improved.

[0056] In addition to the first two steps above, the concentration of the buried channel region may be optimized, and after its formation the gate insulation layer may be heat-treated in an atmosphere containing water vapor, which enables the channel mobility to be improved.

[0057] In addition to any of the above, the gate electrode resistance value may be lowered by:

overlaying a high-melting-point metal silicide layer on the P-type polycrystalline silicon, and, following its formation, heat-treating the gate insulation layer in an atmosphere containing water vapor, which enables the driving power to be improved.

[0058] In addition a further development uses a tungsten, molybdenum or titanium silicide layer, and also, following its formation, heat-treats the gate insulation layer in an atmosphere containing water vapor, which enables the operating speed of the semiconductor device to be improved.

[0059] In addition to any of the above, both hot-carrier resistance and driving power can be improved by providing a region between the buried channel region and the source or drain region having an impurity concentration that is not lower than the impurity concentration of the buried channel region, and not higher than the impurity concentration of the source or drain region, and by, after formation of the gate insulation layer, heat-treating the gate insulation layer in an atmosphere containing water vapor.

[0060] In addition to any of the above, both punch-through resistance and driving power may be improved by providing adjacently beneath the buried channel region, an impurity region of the P-type semiconductor substrate 1 or by optimizing the concentration thereof, and, at the same time, by, following formation of the gate insulation layer, heat-treating the gate insulation layer in an atmosphere containing water vapor.

[0061] In addition to any of the above, channel mobility can be improved by forming the gate insulation layer by using a thermal oxidation method employing dry oxygen followed by heat treatment in an atmosphere containing water vapor.

Claims

1. A method of manufacturing an MIS field-effect transistor including a P-type silicon carbide substrate (1), a gate insulation layer (7) formed on the P-type substrate, a gate electrode (8) formed of P-type polycrystalline silicon on the gate insulation layer (7), an N-type impurity region having an adequate impurity concentration for forming a buried channel region in a semiconductor layer below the gate insulation layer, and transistor-constituting source (5) and drain (6) regions each composed of an N-type impurity region formed respectively adjacent to said gate insulation layer (7) and said gate electrode (8); a depth (Xj) of a junction portion of the source (5) and drain (6) regions being 0.5μm;
   the buried channel region (2) having diffused therein a nitrogen, phosphorus or arsenic impurity having a maximum concentration of 5 x $10^{15}cm^{-3}$ to 1 x $10^{18}cm^{-3}$;
   the gate electrode (8) having boron diffused therein and having an impurity concentration within a range of 1 x $10^{16}cm^{-3}$ to 1 x $10^{21}cm^{-3}$;
   the MIS field-effect transistor having a ratio ($L_{bc} \div Xj$) between a junction depth (L_{bc}) of the buried channel region (2) from an interface between the gate insulation layer (7) and the P-type silicon carbide substrate (1), and the depth (Xj) of the junction portion of the source (5) and drain (6) regions from said interface, which ratio is within a range of not less than 0.2 and not more than 1.0,
   said method comprising:

   forming the buried channel region (2) by using ion implantation of an N-type impurity;
   forming the source region (5) and drain region (6) by using ion implantation at 500°C to implant nitrogen, phosphorus or arsenic at a depth (Xj) of 0.5 μm;
   forming the gate insulation layer (7) by oxidizing the buried channel region (2) at 1200°C for 150 minutes in a gas containing oxygen or for 90 minutes in a gas containing water vapour after the step of forming the buried channel region, source region and drain region, and
   exposing the gate insulation layer (7) to an atmosphere containing water vapour at a temperature of 500°C or more after the step of forming the gate insulation layer.

2. The method according to claim 1, **characterised in that** the gate electrode (8) includes a high melting point metal silicide layer.

3. The method according to any one of claims 1 to 2, **characterised by** causing a region having an impurity concentration within a range of 5 x $10^{16}cm^{-3}$ to 5 x $10^{20}cm^{-3}$, that is not lower than a maximum impurity concentration of an impurity diffusion layer region used to form the buried channel region (2), and not higher than an impurity concentration of the source (5) or drain (6) region to intervene between a region in which the buried channel region (2) is formed and the source (5) or drain (6) region.

4. The method according to any one of claims 1 to 2, **characterised by** including a step of forming a P-type punch-

through prevention region (3), at a depth corresponding to a depth just below the buried channel region, having an impurity concentration that is within a range of 1 x $10^{17}cm^{-3}$ to 1 x $10^{19}cm^{-3}$, and higher than that of the silicon carbide substrate (1), by ion implantation of a P-type impurity element.

Patentansprüche

1. Verfahren zum Herstellen eines MIS-Feldeffekttransistors, der ein p-Typ-Siliciumcarbid-Substrat (1), eine Gate-Isolationsschicht (7), die auf dem p-Typ-Substrat gebildet ist, eine Gate-Elektrode (8), die aus polykristallinem p-Typ-Silicium auf der Gate-Isolationsschicht (7) gebildet ist, einen n-Typ-Störstellenbereich, der eine angemessene Störstellenkonzentration zum Bilden eines innenleitenden Kanalbereichs in einer Halbleiterschicht unter der Gate-Isolationsschicht aufweist, und einen Transistor bildenden Sourcebereich (5) und einen Drainbereich (6) umfasst, die jeweils aus einem n-Typ-Störstellenbereich bestehen, die jeweils benachbart zur Gate-Isolationsschicht (7) und der Gate-Elektrode (8) gebildet sind; wobei eine Tiefe (Xj) eines Übergangsabschnitts des Sourcebereichs (5) und des Drainbereichs (6) 0,5 μm beträgt;
wobei der innenleitende Kanalbereich (2) darin diffundierte Stickstoff-, Phosphor- oder Arsen-Störstellen aufweist, die eine Höchstkonzentration von 5 x 10^{15} cm^{-3} bis 1 x 10^{18} cm^{-3} aufweist;
wobei die Gate-Elektrode (8) darin diffundiertes Bor aufweist und eine Störstellenkonzentration innerhalb eines Bereichs von 1 x 10^{16} cm^{-3} bis 1 x 10^{21} cm^{-3} aufweist;
wobei der MIS-Feldeffekttransistor ein Verhältnis (L_{bc} ÷ Xj) zwischen einer Übergangstiefe (L_{bc}) des innenleitenden Kanalbereichs (2) von einer Grenzfläche zwischen der Gate-Isolationsschicht (7) und dem p-Typ-Siliciumcarbid-Substrat (1) und der Tiefe (Xj) des Übergangsabschnitts des Sourcebereichs (5) und des Drainbereichs (6) von der Grenzfläche aufweist, wobei das Verhältnis in einem Bereich von nicht kleiner als 0,2 und nicht größer als 1,0 liegt, wobei das Verfahren Folgendes umfasst:

   Bilden des innenleitenden Kanalbereichs (2) unter Verwendung einer Ionenimplantation einer n-Typ-Störstelle;
   Bilden des Sourcebereichs (5) und Drainbereichs (6) unter Verwendung von Ionenimplantation bei 500 °C zum Implantieren von Stickstoff, Phosphor oder Arsen in einer Tiefe (Xj) von 0,5 μm;
   nach dem Schritt des Bildens des innenleitenden Kanalbereichs, Sourcebereichs und Drainbereichs, Bilden der Gate-Isolationsschicht (7) durch Oxidieren des innenleitenden Kanalbereichs (2) bei 1200 °C 150 Minuten lang in einem Gas, das Sauerstoff enthält, oder 90 Minuten lang in einem Gas, das Wasserdampf enthält, und nach dem Schritt des Bildens der Gate-Isolationsschicht, Aussetzen der Gate-Isolationsschicht (7) einer Atmosphäre, die Wasserdampf bei einer Temperatur von 500 °C oder höher enthält.

2. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** die Gate-Elektrode (8) eine Metallsilicid-Schicht mit hohem Schmelzpunkt umfasst.

3. Verfahren nach einem der Ansprüche 1 bis 2, **dadurch gekennzeichnet, dass** bewirkt wird, dass ein Bereich, der eine Störstellenkonzentration in einem Bereich von 5 x 10^{16} cm^{-3} bis 5 x 10^{20} cm^{-3} aufweist, die nicht geringer ist als eine maximale Störstellenkonzentration eines Störstellendiffusionsschichtbereichs, der verwendet wird, um den innenleitenden Kanalbereich (2) zu bilden, und nicht höher als eine Störstellenkonzentration des Source- (5) oder Drainbereichs (6) ist, die zwischen einem Bereich, in dem der innenleitende Kanalbereich (2) gebildet wird, und dem Source- (5) oder Drainbereich (6) liegt.

4. Verfahren nach einem der Ansprüche 1 bis 2, **dadurch gekennzeichnet, dass** es einen Schritt des Bildens eines p-Typ-Sperrschichtbereichs (3) in einer Tiefe umfasst, die einer Tiefe unmittelbar unter dem innenleitenden Kanalbereich entspricht, der eine Störstellenkonzentration aufweist, die innerhalb eines Bereichs von 1 x 10^{17} cm^{-3} bis 1 x 10^{19} cm^{-3} liegt und höher ist als diejenige des Siliciumcarbid-Substrats (1), durch Ionenimplantation eines p-Typ-Störstellenelements.

Revendications

1. Procédé de fabrication d'un transistor à effet de champ MIS comprenant un substrat en carbure de silicium de type P (1), une couche d'isolation de grille (7) formée sur le substrat de type P, une électrode de grille (8) formée de silicium polycristallin de type P sur la couche d'isolation de grille (7), une région d'impuretés de type N ayant une concentration d'impuretés adéquate pour former une région de canal enterrée dans une couche semiconductrice sous la couche d'isolation de grille, et les régions de source (5) et de drain (6) constituant le transistor étant chacune

composées d'une région d'impuretés de type N formée respectivement de façon adjacente à ladite couche d'isolation de grille (7) et ladite électrode de grille (8) ; une profondeur (Xj) d'une partie de jonction des régions de source (5) et de drain (6) étant de 0,5 μm ;
la région de canal enterrée (2) dans laquelle est diffusée une impureté d'azote, de phosphore ou d'arsenic ayant une concentration maximale de 5 x 10^{15} cm^{-3} à 1 x 10^{18} cm^{-3} ;
l'électrode de grille (8) ayant du bore diffusé à l'intérieur et ayant une concentration d'impuretés dans une plage de 1 x 10^{16} cm^{-3} à 1 x 10^{21} cm^{-3} ;
le transistor à effet de champ MIS ayant un rapport ($L_{be} \div Xj$) entre une profondeur de jonction (L_{bc}) de la région de canal enterrée (2) depuis une interface entre la couche d'isolation de grille (7) et le substrat en carbure de silicium de type P (1), et la profondeur (Xj) de la partie de jonction des régions de source (5) et de drain (6) de ladite interface, lequel rapport est dans une plage non inférieure à 0,2 et non supérieure à 1,0,
ledit procédé consistant à :

former la région de canal enterrée (2) en utilisant l'implantation ionique d'une impureté de type N ;
former la région de source (5) et la région de drain (6) en utilisant l'implantation ionique à 500°C pour implanter de l'azote, du phosphore ou de l'arsenic à une profondeur (Xj) de 0,5 μm ;
former la couche d'isolation de grille (7) en oxydant la région de canal enterrée (2) à 1200°C pendant 150 minutes dans un gaz contenant de l'oxygène ou pendant 90 minutes dans un gaz contenant de la vapeur d'eau après l'étape de formation de la région de canal enterrée, de la région de source et de la région de drain, et
exposer la couche d'isolation de grille (7) à une atmosphère contenant de la vapeur d'eau à une température de 500°C ou plus après l'étape de formation de la couche d'isolation de grille.

2. Procédé selon la revendication 1, **caractérisé en ce que** l'électrode de grille (8) comprend une couche de siliciure métallique à point de fusion élevé.

3. Procédé selon l'une quelconque des revendications 1 à 2, **caractérisé en ce qu'**il provoque l'intervention d'une région ayant une concentration d'impuretés dans une plage de 5 x 10^{16} cm^{-3} à 5 x 10^{20} cm^{-3}, qui n'est pas inférieure à une concentration d'impuretés maximale d'une région de couche de diffusion d'impuretés utilisée pour former la région de canal enterrée (2), et pas supérieure à une concentration d'impuretés de la région de source (5) ou de drain (6) entre une région dans laquelle est formée la région de canal enterrée (2) et la région de source (5) ou de drain (6).

4. Procédé selon l'une quelconque des revendications 1 à 2, **caractérisé en ce qu'**il comprend une étape de formation d'une région de prévention de perforation de type P (3), à une profondeur correspondant à une profondeur juste en dessous de la région de canal enterrée, ayant une concentration en impuretés qui se trouve dans une plage de 1 x 10^{17} cm^{-3} à 1 x 10^{19} cm^{-3}, et supérieure à celle du substrat en carbure de silicium (1), par implantation ionique d'un élément d'impureté de type P.

FIG. 1

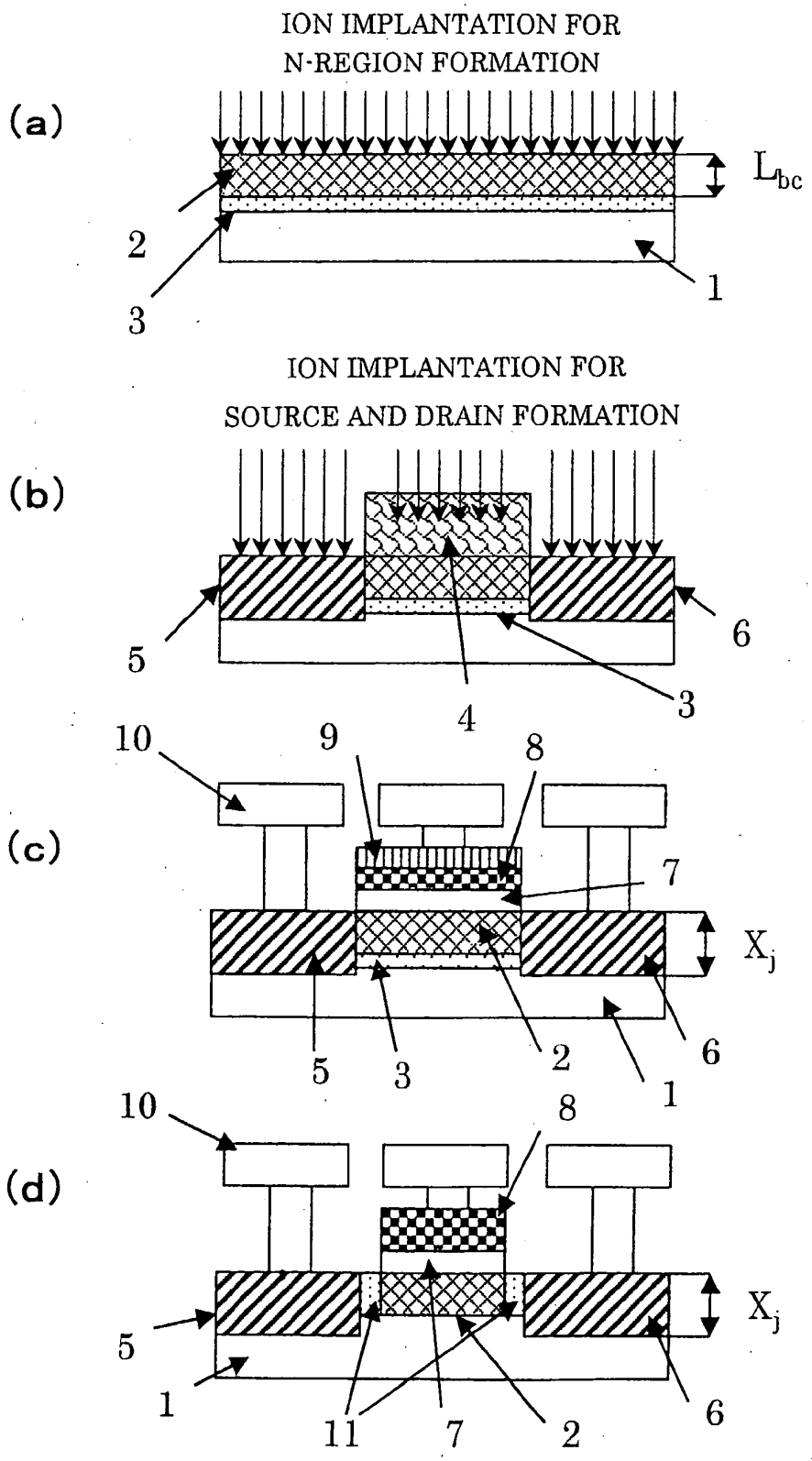

ION IMPLANTATION FOR
N-REGION FORMATION
(a)
L_{bc}
2
3
1
ION IMPLANTATION FOR
SOURCE AND DRAIN FORMATION
(b)
5
6
4
3
10
9
8
(c)
7
X_j
5
3
2
6
1
10
8
(d)
X_j
5
1
11
7
2
6

FIG. 2

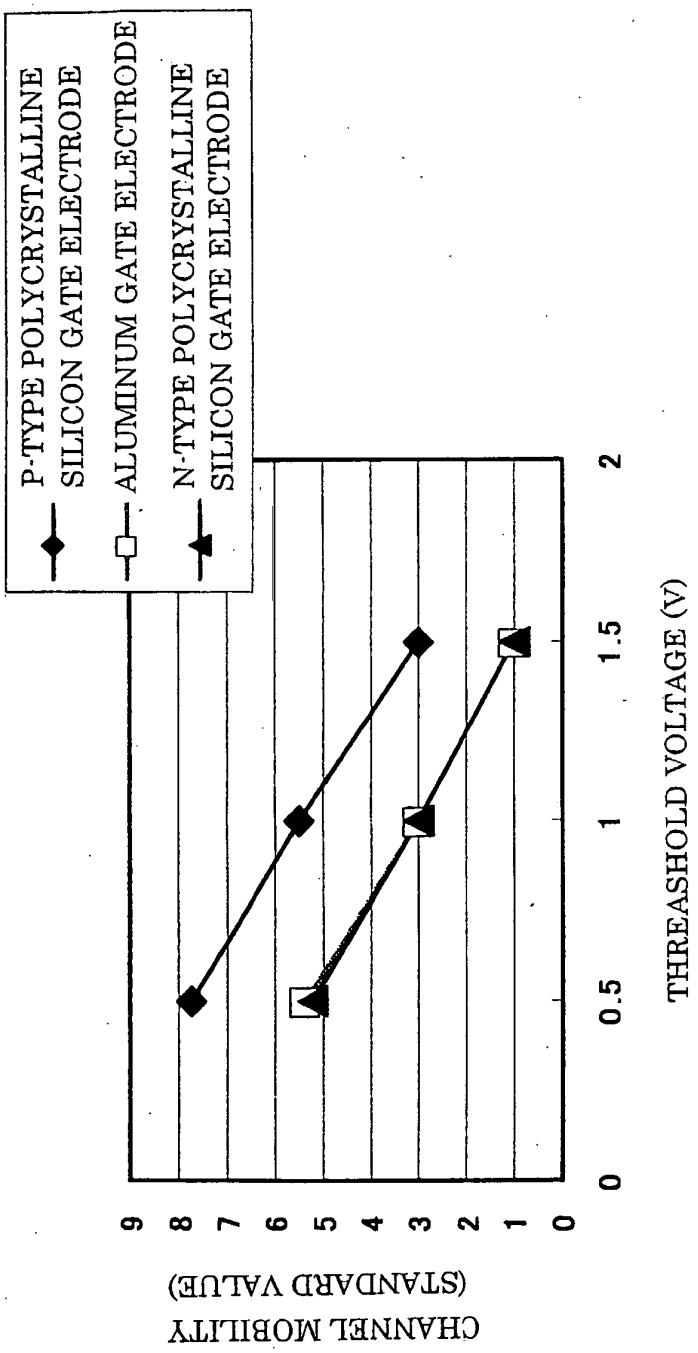

P-TYPE POLYCRYSTALLINE SILICON GATE ELECTRODE
ALUMINUM GATE ELECTRODE
N-TYPE POLYCRYSTALLINE SILICON GATE ELECTRODE
CHANNEL MOBILITY (STANDARD VALUE)
0
1
2
3
4
5
6
7
8
9
THREASHOLD VOLTAGE (V)
0
0.5
1
1.5
2

FIG. 3

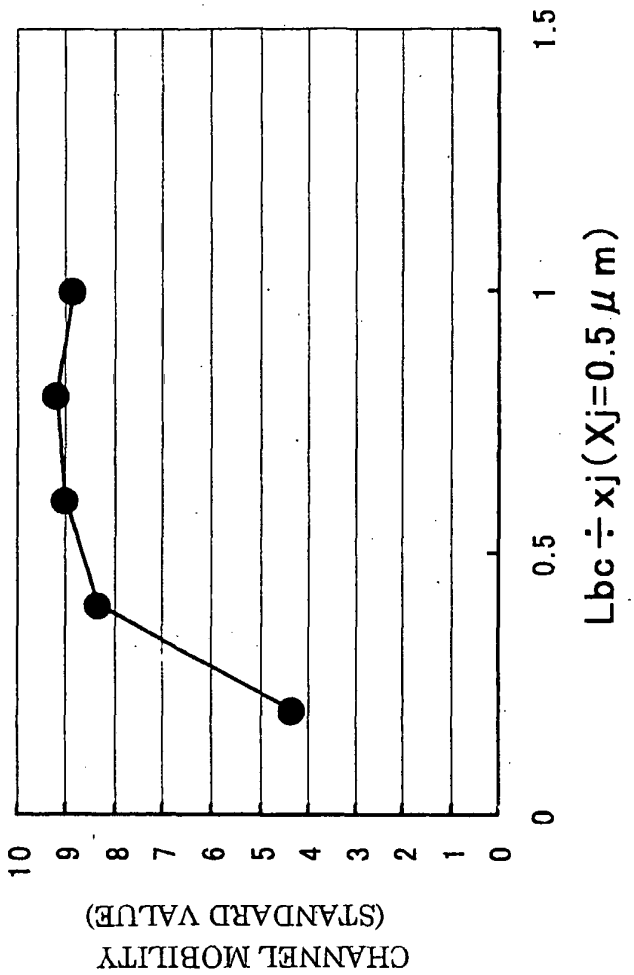

CHANNEL MOBILITY
(STANDARD VALUE)
10
9
8
7
6
5
4
3
2
1
0
0
0.5
1
1.5
Lbc ÷ xj (Xj=0.5 μ m)

FIG. 4

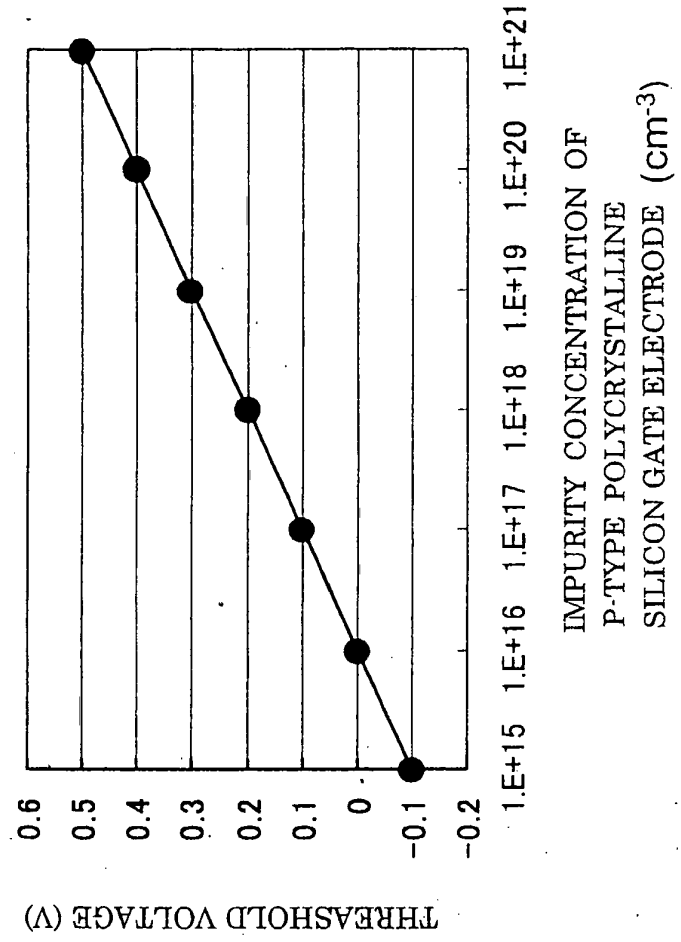
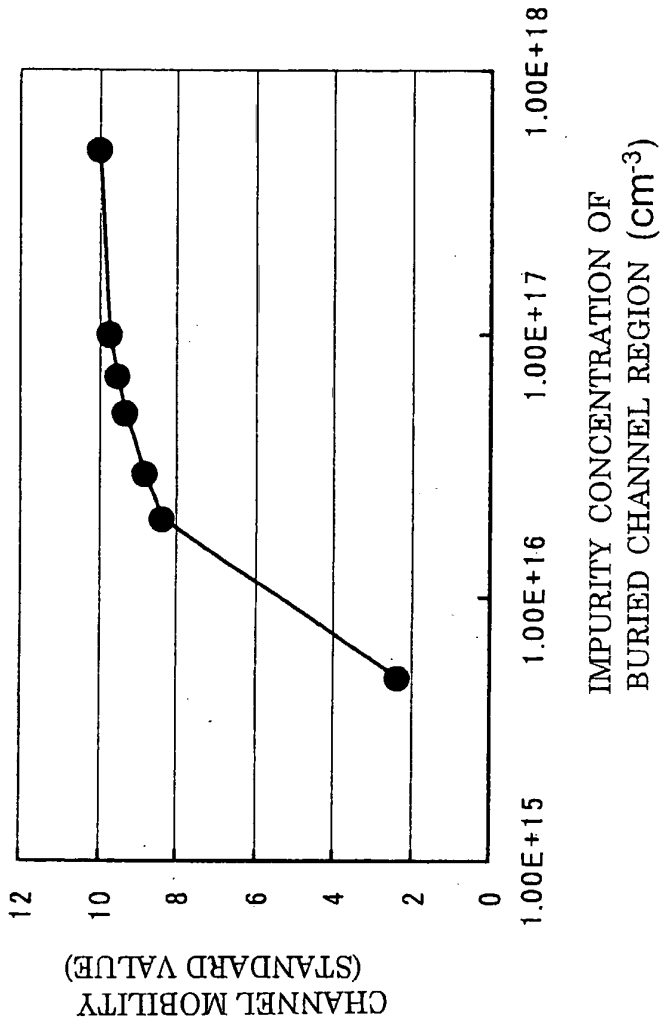

THREASHOLD VOLTAGE (V)
0.6
0.5
0.4
0.3
0.2
0.1
0
-0.1
-0.2
1.E+15
1.E+16
1.E+17
1.E+18
1.E+19
1.E+20
1.E+21
IMPURITY CONCENTRATION OF
P-TYPE POLYCRYSTALLINE
SILICON GATE ELECTRODE (cm-3)

FIG. 5


CHANNEL MOBILITY
(STANDARD VALUE)
12
10
8
6
4
2
0
1.00E+15
1.00E+16
1.00E+17
1.00E+18
IMPURITY CONCENTRATION OF
BURIED CHANNEL REGION (cm-3)

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 5864157 A **[0003]**
- JP HEI8186179 A **[0004]**
- JP HEI7131016 A **[0005]**
- US 5972801 A **[0006]**
- JP HEI5129596 A **[0007] [0008]**
- US 5151759 A **[0010]**

Non-patent literature cited in the description

- High Temperature Performance of NMOS Integrated Inverters and Ring Oscillators. *6H-SiC-IEEE Transactions on Electron Devices,* April 2000, vol. 47 (4 **[0009]**
- Insulator Investigation on SiC for Improved Reliability. *IEEE Transactions on Electronic Devices,* March 1999, vol. 46 (3), 525-532 **[0011]**