Novel Electron Transport in Nanocrystalline Silicon

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Future microelectronics technology requires a reduction in both the lateral and vertical dimensions of silicon devices into the nanometer regime. Silicon materials where the nanostructure is tailored chemically can meet the requirements for advanced nanoscale devices such as quantum dots and single-electron transistors (SETs). One promising material is nanocrystalline silicon (nc-Si), which contains silicon grains with sizes that can be controlled down to 5 nm, embedded in an amorphous silicon (a-Si:H) matrix. This may be used to naturally form charging islands in SETs. In this project, we have studied the relationship between the film microstructure and the electric characteristics of SETs fabricated in nc-Si.

We fabricated side-gated nanowire SETs using nc-Si films prepared by 100 MHz-VHF PECVD and using polycrystalline silicon (poly-Si) films prepared by solid-phase-crystallization (SPC). The films were 50 nm thick, deposited on a buried oxide layer grown on a crystalline silicon substrate. We characterized the dependence of electron transport in the nc-Si on the physical dimensions of the conducting channel using nanowires of different dimensions or using point-contacts (Fig. 1). In addition, we investigated the effect of defect density on the electrical characteristics by modifying the film structure using annealing at 1000°C in oxygen or argon. We have also characterized the film structure using transmission electron microscopy (TEM), Raman spectroscopy and electron spin resonance.

The Raman spectrum and TEM analysis demonstrate that the nc-Si films is composed of ~70% crystalline silicon and ~30% amorphous silicon, and the grain size ranges from 4 nm to 8nm. This suggests that the crystalline grains are surrounded by ~0.5 nm-thick amorphous silicon tissues on average. We observed Coulomb blockade up to 16 K in SETs using nanowires of 50 nm width and 1 μm length. SETs using 30 nm × 30 nm point-contacts also exhibit Coulomb blockade (Fig. 2), which persists up to 58 K (Fig. 3). These results indicate that a narrower channel limits electron transport paths better and helps to achieve higher temperature operation. However, activation energy measurements to evaluate the barrier height indicate that the tunnelling barrier height at maximum is ~40 meV (Fig. 4), which is not enough for high temperature operation. In addition, it is found that the transport mechanism changes from a thermally-assisted tunnelling process to percolation conduction at a transition temperature of T_1 = ~60 K.

We also observed Coulomb blockade effects in annealed nanowire and oxidized nanowire SETs. We compare these results with those obtained in SETs fabricated in poly-Si. In poly-Si SETs, only oxidized nanowires exhibited Coulomb blockade. These results suggest that the grain boundary structure is very different between nc-Si and poly-Si. In nc-Si, the grain boundary consists of amorphous silicon, which forms the tunnelling barrier. If the nc-Si is annealed, dangling bonds increase due to hydrogen effusion from grain boundaries. These bonds trap electrons and form tunnelling barriers. In contrast, poly-Si prepared by SPC at 850°C has far smaller amounts of hydrogen and amorphous silicon at the grain boundaries and the associated potential barrier is not high enough to confine electrons. Oxidation of grain boundaries can form the tunnelling barrier in these devices.

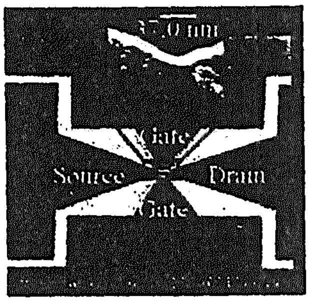

Fig. 1. Scanning electron micrograph of a point-contact SET. Channel size is 30 nm × 30 nm.

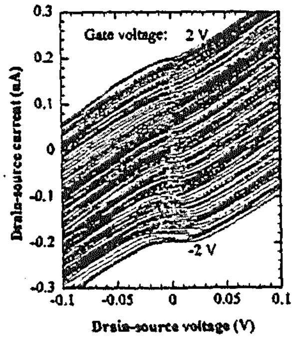

Fig. 2. Source-drain I-V characteristics of nc-Si SET at 8 K.

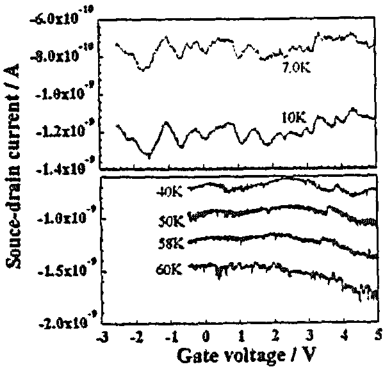

Fig. 3 Current oscillations as a function of gate voltage in a nc-Si SET. The temperature is varied from 7 to 60 K.

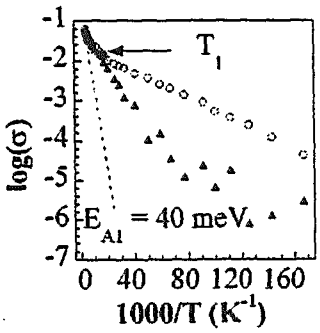

Fig. 4 Temperature dependence of dark conductivity in a nc-Si SET. Circles: outside Coulomb gap. Triangles: inside Coulomb gap.

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