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(54) FIELD-EFFECT TRANSISTOR WITH SPIN-DEPENDENT TRANSMISSION CHARACTERISTIC WITH HALF-METAL SOURCE AND DRAIN

FELDEFFEKTTRANSISTOR MIT SPINABHÄNGIGER ÜBERTRAGUNGSEIGENSCHAFT MIT HALBMETALLISCHEM SOURCE UND DRAIN

TRANSISTOR A EFFET DE CHAMP A PROPRIETES DE TRANSMISSION DEPENDANT DE SPIN AVEC SOURCE ET DRAIN SEMI-MÉTALLIQUE

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to novel transistors, and more particularly, to a field-effect transistor with spin-dependent transmission characteristics and a nonvolatile memory using the field-effect transistor.

BACKGROUND OF THE INVENTION

[0002] Today's highly advanced information society has dramatically developed, and particularly, "mobile communication devices" are being widely spread in the general public. The great demand for "mobile communication devices" is regarded as one of the essential elements in the future semiconductor industry. To satisfy the demand, however, it is necessary to achieve nonvolatility of information, as well as high-speed performance, lower electric consumption, and large capacities that have conventionally be required in semiconductor integrated circuits. In response to such demands, attention has been drawn to a novel memory device in which the ferromagnetic storage technique that excels in nonvolatile high-density recording combined with the semiconductor integration electronics. This device is called a magnetic random access memory (hereinafter referred to as "MRAM"), and a magnetic tunnel junction (hereinafter referred to as "MTJ") having a thin insulating tunnel barrier sandwiched between ferromagnetic electrodes is used as a memory device for the MRAM (disclosed in "Present and Future of Magnetic RAM Technology", K. Inomata, IEICE Trans. Electron. Vol.E84-C, pp. 740-746, 2001, for example).

[0003] In the MTJ, the tunneling resistance differs depending on the relative magnetization direction between the ferromagnetic electrodes. This is called a tunneling magneto-resistance (TMR) effect. Utilizing TMR, it is possible to electrically detect the magnetizing state of each ferromagnetic body. Accordingly, the information nonvolatile storage technique using ferromagnetic bodies can be ideally incorporated into the semiconductor integration electronics by virtue of the MTJ.

[0004] In the following, an example of the conventional technique is described in conjunction with Fig. 10. As shown in Fig. 10, in a MRAM memory cell 100, a 1-bit memory cell is formed with a MTJ 101 and a metal-oxide-semiconductor field-effect transistor (hereinafter referred to as "MOSFET") 103. The MTJ 101 is a tunnel junction that is formed with a first ferromagnetic electrode 105, a second ferromagnetic electrode 107, and a tunnel barrier (an insulator) 108 formed with an insulator provided between the first and second ferromagnetic electrodes 105 and 107.

[0005] The source (S) of the MOSFET 103 is grounded (GND), and the drain (D) of the MOSFET 103 is connected to the ferromagnetic electrode 107 of the MTJ 101 with a plug PL or the like. The ferromagnetic electrode 105 of the MTJ 101 is connected to a bit line BL. A rewrite word line 111 is disposed to cross the bit line BL immediately above or below the MTJ 101, being electrically insulated from the MTJ 101 and the other lines by the insulating film 115. A read word line WL is connected to the gate electrode G of the MOSFET 103.

[0006] Since the magnetization direction can be maintained in a non-volatile manner in a ferromagnetic body, binary information can be stored in a non-volatile manner by adjusting the relative magnetization state between the ferromagnetic electrodes of the MTJ to parallel magnetization or antiparallel magnetization. In the MTJ, the tunneling resistance differs depending on the relative magnetization state between the two ferromagnetic electrodes, due to the TMR effect. Accordingly, the magnetization state in the MTJ can be electrically detected, using the tunneling resistance that depends on the magnetization state such as parallel magnetization and antiparallel magnetization.

[0007] To rewrite information, the retentivity of the ferromagnetic electrode 105 is made different from the retentivity of the ferromagnetic electrode 107 in the MTJ 101, or the magnetization of the ferromagnetic electrode with lower retentivity or an unfixed magnetization direction is inverted while the magnetization direction of the other ferromagnetic electrode is fixed. Hereinafter, the ferromagnetic electrode having the magnetization varied will be referred to as the "free layer", and the ferromagnetic electrode having the fixed magnetization will be referred to as the "pin layer". More specifically, currents are applied to the bit line BL and the rewrite word line 111 that cross each other on the selected cell, and the magnetization state of the MTJ 101 in the memory cell 100 selected by the compound magnetic field of the magnetic fields induced by the currents is changed to parallel magnetization or antiparallel magnetization. Here, the size of each current to be applied to each corresponding line is set so that the magnetization of each MTJ 101 of the unselected cells having the same bit line BL or the rewrite word line 111 as that of the selected cell is not inverted by the magnetic fields generated from only either the bit line BL or the rewrite word line 111. To read information, a voltage is applied to the read word lines WL connected to the selected cell so as to energize the MOSFET 103, and a read driving current is then applied to the MTJ 101 via the bit line BL. In the MTJ 101, the tunneling resistance differs depending on the magnetization state such as parallel magnetization or antiparallel magnetization, due to the TMR effect. Accordingly, the magnetization state can be checked by detecting a voltage drop (hereinafter referred to as "output voltage") caused by the read driving current in the MTJ 101 (see "Present and Future of Magnetic RAM Technology", K. Inomata, IEICE Trans. Electron. Vol.E84-C, pp. 740-746, 2001).

SUPRIYO DATTA ET AL: "ELECTRONIC ANALOG OF THE

[0008] ELECTRO-OPTIC MODULATOR" Applied Physics Letters, AIP, American Institute of Physics, Melville, NY, US, vol. 56, no. 7, 12 February 1990, pages 665-667, XP000126701, ISSN: 0003-6951 discloses an electron wave analog of an electro-optic light modulator having two metal contacts with an InAlAs layer therebetween on a InGaAs substrate. A Schottky gate is provided on the InAlAs layer.

[0009] WO 01/99137 discloses atomically ordered interfaces between semiconductor and ferromagnetic materials to provide spin filters. The spin filters may be used to inject strongly spin polarized currents into a semiconductor for use in spintronic devices.

[0010] SCHMIDT G ET AL: "Spin injection into semiconductors, physics and experiments" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, IOP, BRISTOL, GB, vol. 17, no.4, April 2002, pages 310-321, XP002210978, ISSN: 0268-1242 discloses a spin injection device consisting of a non-magnetic semiconductor layer with two Dilute magnetic semiconductor (DMS) top-contacts.

[0011] US 6,381,171 discloses a spin-dependent tunneling effect element which offers the spin accumulation effect at room temperature while also providing a data storage or "memory" element and magnetic reading head each using the tunnel effect element. A magnetic element comprises first and second ferromagnetic layers and a layer of semiconductor particles neighbouring the first ferromagnetic layer with a first tunnel barrier disposed between them and also neighbouring the second ferromagnetic layer with a second tunnel barrier laid therebetween.

[0012] US 5,416,353 discloses a magnetoresistance effect element that is prepared by successively forming one upon the other, a first magnetic layer, a P- or N-type semiconductor layer, a second magnetic layer, and a magnetization fixing layer on an insulating substrate. A Schottky junction is formed between the first magnetic layer and the semiconductor layer and between the semiconductor layer and the second magnetic layer.

DISCLOSURE OF THE INVENTION

[0013] A MTJ has a binary resistance value that depends on whether the magnetization state between the ferromagnetic electrodes opposed to each other via a tunnel barrier is parallel magnetization or antiparallel magnetization. To accurately detect the binary information with a driving current, it is necessary to optimize the size of the output voltage through adjustment of the impedance (the junction resistance) of the MTJ.

[0014] To accurately read the contents of stored information, the ratio of output signals between the two magnetization states of parallel magnetization and antiparallel magnetization needs to be high. Therefore, it is necessary to maximize the rate of change in TMR between the case where the MTJ exhibits parallel magnetization and the case where the MTJ exhibits antiparallel magnetization. The MTR ratio depends on the spin polarization rate P of the ferromagnetic electrodes. To increase the TMR ratio, a ferromagnetic material with a high P value needs to be employed for the ferromagnetic electrodes.

[0015] The TMR ratio in a MTJ greatly depends on the bias voltage to be applied to the MTJ, and rapidly decreases according to the bias voltage. When a high driving current is applied to the MTJ to read information with high precision and at a high speed, the voltage drop becomes large in the MTJ, and the TMR ratio decreases accordingly. Therefore, bias resistance is required for the TMR ratio, so as to prevent the TMR ratio from decreasing even if a large voltage drop is caused in the MTJ.

[0016] A MRAM is suitable for high-density integration, having a simple structure. Also, a MRAM is desirable because each MTJ can be reduced to a nanoscale structure. When high integration of several gigabits or higher is to be realized, the channel length of the MOSFET is expected to be 0.1 μm or shorter. However, if minute MTJs are integrated in conformity with such minute transistors, the contacts and multilayer lines take up a large portion of the cell area, and high-density integration of both components becomes difficult. Therefore, there is a demand for memory cells with simpler structures.

[0017] The present invention provides a transistor using spin-polarized conduction carriers according to claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Fig. 1 is a cross-sectional view schematically illustrating the structure of a MISFET in accordance with a first embodiment of the present invention;

Fig. 2A shows the energy band structure of the ferromagnetic source, the semiconductor layer, and the ferromagnetic drain of a MISFET of the accumulation n-channel type that employs a ferromagnetic metal for the ferromagnetic source and the ferromagnetic drain in the structure of Fig. 1;

Fig. 2B shows the energy band structure of the ferromagnetic source, the semiconductor layer, and the ferromagnetic drain of a MISFET of the inversion n-channel type;

Fig. 3A shows the energy band structure of the ferromagnetic source, the semiconductor layer, and the ferromagnetic drain of a MISFET of the accumulation n-channel type that employs a half metal for the ferromagnetic source and the ferromagnetic drain in a structure in accordance with a second embodiment of the present invention;

Fig. 3B shows the energy band structure of the ferromagnetic source, the semiconductor layer, and the ferromagnetic drain of a MISFET of the inversion n-channel type in the structure in accordance with the second embodiment;

Fig. 4A illustrates the principles of the operation of a MISFET having the energy band structure shown in Fig. 2A, and shows the energy band structure in a case of parallel magnetization;

Fig. 4B shows the energy band structure that is obtained when a bias V_{DS} is applied in the case where the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization;

Fig. 4C shows the energy band structure that is obtained when a bias V_{GS} is further applied in the situation shown in Fig. 4B;

Fig. 4D shows the energy band structure that is obtained in a case where the ferromagnetic source and the ferromagnetic drain exhibit antiparallel magnetization with the same bias as that of Fig. 4C;

Fig. 5A illustrates the principles of the operation of a MISFET having the energy band structure shown in Fig. 2B, and shows the energy band structure in a case of parallel magnetization;

Fig. 5B shows the energy band structure that is obtained when a bias V_{DS} is applied in the case where the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization;

Fig. 5C shows the energy band structure that is obtained when a bias V_{GS} is further applied in the situation shown in Fig. 5B;

Fig. 5D shows the energy band structure that is obtained in a case where the ferromagnetic source and the ferromagnetic drain exhibit antiparallel magnetization with the same bias as that of Fig. 5C;

Fig. 6A illustrates the principles of the operation of a MISFET having the energy band structure shown in Fig. 3A, and shows the energy band structure in a case of parallel magnetization;

Fig. 6B shows the energy band structure that is obtained when a bias V_{DS} is applied in the case where the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization;

Fig. 6C shows the energy band structure that is obtained when a bias V_{GS} is further applied in the situation shown in Fig. 6B;

Fig. 6D shows the energy band structure that is obtained in a case where the ferromagnetic source and the ferromagnetic drain exhibit antiparallel magnetization with the same bias as that of Fig. 6C;

Fig. 7A illustrates the principles of the operation of a MISFET having the energy band structure shown in Fig. 3B, and shows the energy band structure in a case of parallel magnetization;

Fig. 7B shows the energy band structure that is obtained when a bias V_{DS} is applied in the case where the ferromagnetic source and the ferromagnetic drain exhibit parallel magnetization;

Fig. 7C shows the energy band structure that is obtained when a bias V_{GS} is further applied in the situation shown in Fig. 7B;

Fig. 7D shows the energy band structure that is obtained in a case where the ferromagnetic source and the ferromagnetic drain exhibit antiparallel magnetization with the same bias as that of Fig. 7C;

Fig. 8 schematically shows the drain current-voltage characteristics of the source ground of a MISFET in accordance with this embodiment;

Fig. 9A illustrates an example structure of a memory circuit that employs MISFETs in accordance with this embodiment;

Fig. 9B illustrates a memory circuit that has an output terminal V_o connected to the bit line end of the memory circuit of Fig. 9A, and is connected to a supply voltage V_{DD} via a load R_L branching from the output terminal V_o;

Fig. 9C shows the static characteristics and operating points of the memory cell of Fig. 9B;

Fig. 10 is a cross-sectional view of a memory cell that is used in a conventional MRAM;

Fig. 11 illustrates an example structure of a memory cell in accordance with any of the embodiments of the present invention, in which a ferromagnetic source is shared;

Fig. 12 shows the energy band structure of a MISFET in accordance with an example useful for understanding the present invention;

Fig. 13A shows the energy band structure of a MISFET in which an n-type ferromagnetic semiconductor is used for the source and the drain, and an intrinsic semiconductor is interposed between the source and the drain; and

Fig. 13B shows the energy band structure of a MISFET in which an n-type ferromagnetic semiconductor is used for the source and the drain, and a p-type semiconductor is interposed between the source and the drain.

DESCRIPTION OF THE PREFERRED EMBODIMENTS AND EXAMPLES

[0019] A metal-insulator-semiconductor field-effect transistor (hereinafter referred to as "MISFET") in accordance with the present invention stores information as the relative magnetization direction of a drain made of a ferromagnetic body with respect to a source made of a ferromagnetic body (hereinafter referred to as "ferromagnetic drain" and "ferromagnetic source"), and reads the stored information utilizing the transmission characteristics depending on the relative magnetization direction. With such a MISFET in accordance with the present invention, a single transistor can form a 1-bit non-volatile memory cell. Accordingly, a high-speed, high-capacity non-volatile memory can be produced.

[0020] First, a MISFET in accordance with a first embodiment of the present invention is described, with reference to the accompanying drawings.

[0021] Fig. 1 is a cross-sectional view of the MISFET in accordance with the first embodiment of the present invention. As shown in Fig. 1, the MISFET of this embodiment includes a MIS structure that is the same as that of a general MISFET (a SiMOSFET, for example) that is formed with a gate electrode 7, a gate insulating film 11, and a non-magnetic semiconductor layer 1, and a source (a ferromagnetic source) 3 and a drain (a ferromagnetic drain) 5 that form a Schottky junction with the non-magnetic semiconductor film 1. According to the invention, the ferromagnetic source and the ferromagnetic drain is made of a half metal such as Heusler alloy such as Co_2MnSi, zinc-blende CrAs, CrSb, and MnAs. The ferromagnetic source 3 and the ferromagnetic drain 5 are formed by epitaxially growing or depositing a ferromagnetic material on the non-magnetic semiconductor layer 1. Alternatively, the ferromagnetic source 3 and the ferromagnetic drain 5 may be formed by introducing magnetic atoms into the non-magnetic semiconductor layer 1 through thermal diffusion or ion implanting. The arrows shown on the ferromagnetic source and the ferromagnetic drain in Fig. 1 indicate the magnetization direction. The gate insulating film may be made of SiO_2, Al_2O_3, or HfO_2, which is a high dielectric constant material.

[0022] In the MISFET of this embodiment, a carrier of the same conduction type as the non-magnetic semiconductor layer (or a semiconductor substrate) 1 can be made a conduction carrier. Alternatively, a carrier of the opposite conduction type to the non-magnetic semiconductor layer 1 may be induced and used as a conduction carrier. Here, the former is referred to as an accumulation channel type, and the latter is referred to as an inversion channel type, for ease of explanation. In a case where an n-channel MISFET is formed, an n-type semiconductor is used for the accumulation channel type, while a p-type semiconductor is used for the inversion channel type. Likewise, in a case where a p-channel MISFET is formed, a p-type semiconductor is used for the accumulation channel type, while an n-type semiconductor is used for the inversion channel type. Hereinafter, an n-channel accumulation channel type will be referred to as an accumulation n-channel type, and an n-channel inversion channel type will be referred to as an inversion n-channel type. Likewise, a p-channel accumulation channel type will be referred to as an accumulation p-channel type, and a p-channel inversion channel type will be referred to as an inversion p-channel type.

[0023] Regardless of whether or not a channel actually exists, the semiconductor region immediately below the interface between the gate insulating film and the semiconductor is referred to as a channel region. In the following, the energy band structures of a transistor of the accumulation n-channel type and a transistor of the inversion n-channel type are described with respect to a case where a ferromagnetic metal is used for the ferromagnetic source and the ferromagnetic drain, and a case where a half metal is used for the ferromagnetic source and the ferromagnetic drain. Although not described in detail, a MISFET of the accumulation p-channel type and a MISFET of the inversion p-channel type can be formed in the same manner as described below. In accordance with the present invention, enhancement-type MISFETs and depression-type MISFETs can be formed. In the following, enhancement-type MISFETs will be described. Originally, the term "spin" is used as in "spin angular momentum". In the following description, however, electrons with up spins may be referred to simply as "up spins" in terms of carriers.

[0024] Figs. 2A and 2B show energy band structures in the case where a ferromagnetic metal is employed as the ferromagnetic body, examples not forming part of the claimed invention. Figs. 3A and 3B show energy band structures, according to the invention, where a half metal is employed as the ferromagnetic body.

[0025] Fig. 2A shows the energy band structure in the vicinity of the channel region of a MISFET of the accumulation n-channel type in the case where a ferromagnetic metal is used for the ferromagnetic source and the ferromagnetic drain. The ferromagnetic source 3 and the ferromagnetic drain 5 are formed by Schottky junction the non-magnetic n-type semiconductor layer 1 to the ferromagnetic metal (3, 5). The solid lines on the ferromagnetic source 3 and the ferromagnetic drain 5, and the dotted line on the n-type semiconductor layer 1 in Fig. 2A indicate Fermi energy E_F. E_G indicates the band gap of the semiconductor.

[0026] E_C and E_V indicate the bottom of the conduction band of the semiconductor layer 1 and the top of the valence band, respectively. In the drawings hereafter, E_F, E_C, E_V, and E_G indicate the same as above. The height of the barrier of the Schottky junction between the ferromagnetic metal and the n-type semiconductor is denoted by ϕ_n, which represents the energy difference between the Fermi energy E_F and the energy E_C at the bottom of the conduction band of the n-type semiconductor layer 1 on the junction interface. The arrows shown over the Fermi energy of the ferromagnetic source 3 and the ferromagnetic drain 5 indicate the direction of majority spins. An upward arrow indicates up spins, and a downward arrow indicates down spins. It should be noted that minority spins are not shown in the drawings. In the following cases where ferromagnetic metal is used, the direction of the majority spins is shown in the band structure.

[0027] Fig. 2B shows the energy band structure in the vicinity of the channel region of a MISFET of the inversion n-channel type in the case where a ferromagnetic metal is used for the ferromagnetic source and the ferromagnetic drain. The ferromagnetic source 3 and the ferromagnetic drain 5 made of the ferromagnetic metal and the p-type semiconductor layer 1 form a Schottky junction. The height of the barrier of the Schottky junction between the ferromagnetic metal and the p-type semiconductor is denoted by ϕ_p, which represents the energy difference between the Fermi energy E_F and the energy E_V at the top of the valence band of the p-type semiconductor layer 1 on the junction interface. The energy difference between the Fermi energy E_F and the energy E_C at the bottom of the conduction band of the p-type semiconductor layer 1 on the junction interface is denoted by ϕ_n.

[0028] Next, a MISFET in accordance with a second embodiment of the present invention is described, with reference to the accompanying drawings.

[0029] Fig. 3A illustrates a MISFET in accordance with this embodiment, and shows the energy band structure in the vicinity of the channel region of a MISFET of the accumulation n-channel type, where according to the invention a half metal is used for the ferromagnetic source and the ferromagnetic drain. A half metal exhibits a metallic band structure (hereinafter referred to as the "metallic spin band") for one direction of spins, while exhibiting a semiconductor (or insulating) band structure (hereinafter referred to as the "semiconductor spin band") for the opposite spins. With a half metal, a half-occupied band for one spin is provided, and a fully-occupied band (a valence band) is separated for the other spin from an empty band (a conduction band) by a band gap. Accordingly, the Fermi energy E_F crosses the metallic spin band of one spin, but crosses the band gap with respect to the other spin. The carrier conduction is realized only by the spin belonging to the metallic spin band.

[0030] In Fig. 3A, the solid line shown in the middle of each of a ferromagnetic source 3a and a ferromagnetic drain 5a indicates the Fermi energy E_F. Accordingly, E_F also represents the Fermi surface of the metallic spin band. The solid lines E_C^{HM} and E_V^{HM} represent the bottom of the conduction band in the semiconductor spin band and the top of the valence band, respectively. The band gap of the semiconductor spin band of the half metal (3a, 5a) is denoted by E_G^{HM}. In the case where a MISFET of the accumulation n-channel type is formed with the half metal (3a, 5a), the metallic spin band of the half metal (3a, 5a) and the n-type semiconductor layer 1 need to form a Schottky junction with a barrier height ϕ_n. With the junction, the bottom of the conduction band of the semiconductor spin band of the half metal (3a, 5a) exhibits higher energy than the bottom of the conduction band of the n-type semiconductor layer 1, and preferably forms an energy discontinuity ΔE_C at the interface.

[0031] An energy discontinuity ΔE_V represents the energy difference between the energy at the top of the valence band of the semiconductor spin band in the half metal (3a, 5a) and the energy at the top of the valence band of the n-type semiconductor layer 1 at the junction interface. In the following cases, the energy discontinuities at the junction interface between the semiconductor layer 1 and the conduction and valence bands in the semiconductor spin band are denoted by ΔE_C and ΔE_V in the case where a half metal is employed for the ferromagnetic source and the ferromagnetic drain.

[0032] In the drawing, the Fermi energy of non-magnetic contacts 3b and 5b joined to the ferromagnetic source 3a and the ferromagnetic drain 5a made of the half metal is also shown. Accordingly, in the case of employing a half metal, the ferromagnetic source 3 is formed with the ferromagnetic source 3a and the non-magnetic contact 3b. The same applies to the ferromagnetic drain. Hereinafter, if the ferromagnetic source 3 and the ferromagnetic drain 5 are described without specifying whether they are made of a ferromagnetic metal or a half metal, the ferromagnetic source 3 and the ferromagnetic drain 5 include the ferromagnetic source 3a and the ferromagnetic drain 5. The energy difference between the Fermi energy E_F of the non-magnetic contacts 3b and 5b and the conduction band E_C^{HM} in the semiconductor spin band is denoted by ϕ_n'.

[0033] Fig. 3B shows the energy band structure in the vicinity of the channel region of a MISFET of the inversion n-channel type in the case where a half metal is used for the ferromagnetic source and the ferromagnetic drain.

[0034] The ferromagnetic source 3a and the ferromagnetic drain 5a need to be formed by Schottky junction the p-type semiconductor layer 1 to the metallic spin band of the half metal. The height of the Schottky junction barrier between the metallic spin band of the half metal (3a, 5a) and the p-type semiconductor layer 1 is denoted by ϕ_p. The energy difference between the Fermi energy E_F in the half metal (3a, 5a) and the energy E_C at the bottom of the conduction band of the p-type semiconductor layer 1 at the junction interface is denoted by ϕ_n. The bottom of the conduction band of the semiconductor spin band of the half metal (3a, 5a) exhibits higher energy than the bottom of the conduction band of the p-type semiconductor layer 1, and preferably forms an energy discontinuity ΔE_C at the interface.

[0035] The difference between the Fermi energy and the energy E_C^{HM} at the bottom of the conduction band of the semiconductor spin band in the half metal (3a, 5a) is denoted by ϕ_n'. The difference between the Fermi energy and the energy E_V^{HM} at the top of the valence band of the semiconductor spin band in the half metal (3a, 5a) is denoted by ϕ_p'.

[0036] In the following, the principles of the operation of each MISFET in accordance with this embodiment are described, with reference to the accompanying drawings. In each MISFET in accordance with this embodiment, the ferromagnetic source functions as a spin injector that inject spins to the channel, while the ferromagnetic drain functions as a spin analyzer that detects, as en electric signal, the orientation of the spins of conduction carriers injected to the channel. Below, in order to simplify the explanations, examples will be shown that employ either a ferromagnetic metal or a half metal for the ferromagnetic source and the ferromagnetic drain, as described above. Further, it is possible to use a ferromagnetic metal for one of the ferromagnetic source and the ferromagnetic drain, and a half metal for the other one of the ferromagnetic source and the ferromagnetic drain.

[0037] According to the invention, however, both the ferromagnetic source and the ferromagnetic drain must be made of half-metals.

[0038] Hereinafter, the situation in which the relative magnetization direction of the ferromagnetic drain is the same as that of the ferromagnetic source will be referred to as "parallel magnetization", and the situation in which the relative magnetization direction of the ferromagnetic drain is opposite to that of the ferromagnetic source will be referred to as "antiparallel magnetization". The channel length of each MISFET is sufficiently shorter than the spin relaxation length, and the Rashba effect due to a gate voltage should be ignored.

[0039] Referring now to Figs. 4A through 4D, the principles of the operation of a MISFET of the accumulation n-channel type using a ferromagnetic metal for the ferromagnetic source and the ferromagnetic drain are described. Fig. 4A shows an energy band structure in the parallel state, and corresponds to Fig. 2A.

[0040] In the parallel state shown in Fig. 4A, a bias V_{GS} (=0) is applied between the ferromagnetic source 3 and the gate electrode 7, and a bias V_{DS} is applied between the ferromagnetic source 3 and the ferromagnetic drain 5. The bias V_{DS} is then divided between the Schottky junction of the ferromagnetic source 3 and the Schottky junction of the ferromagnetic drain 5, and accordingly, the potential shown in Fig. 4B is obtained. The Schottky junction of the ferromagnetic drain 5 is forward-biased, and the height of the Schottky barrier on the drain side, seen from the bottom of the conduction band of the center portion of the channel, decreases (or disappears). On the other hand, the Schottky junction of the ferromagnetic source 3 is reverse-biased, and the height of the Schottky barrier on the source side, seen from the bottom of the conduction band of the center portion of the channel, increases. Here, the bias V_{DS} is applied in such a manner that the Fermi energy E_F crosses the band edge of the Schottky barrier on the source side, but the bias V_{DS} is of such a size as to hardly cause a current through a tunneling effect. Accordingly, the distance d between the Schottky junction interface on the source side and the crossing point of the Fermi energy of the ferromagnetic source 3 and the band edge of the Schottky barrier is adequately thick so that a carrier tunneling effect is not caused in the channel from the ferromagnetic source 3. Since the Schottky junction on the source side is reverse-biased, a current almost equivalent to a reverse saturation current of the Schottky junction due to the carriers thermally beyond the barrier with a height ϕ_n is generated from the ferromagnetic source 3. However, the current can be sufficiently restricted and made smaller by properly adjusting the height ϕ_n. Accordingly, the MISFET is put into a shut-off state, when the bias V_{GS} is 0.

[0041] Next, the bias V_{GS} (>0) is applied to the gate electrode 7. The electric field in the vicinity of the Schottky barrier on the source side is intensified by the line of electric force directed from the gate electrode 7 to the ferromagnetic source 3. The width of the Schottky barrier decreases as shown in Fig. 4C (indicated by d'). Accordingly, the conduction electrons of the ferromagnetic source 3 pass through the potential barrier by virtue of a tunneling effect, and are injected to the channel region immediately below the gate insulating film 11. At this point, majority spins and minority spins are injected from the ferromagnetic source 3. Since the carrier density of the majority spins is higher than that of the minority spins, the injected electrons are spin-polarized. The spin polarization rate of the injected electrons depends on the spin polarization rate in the vicinity of the Fermi energy. As the spin polarization rate in the vicinity of the Fermi energy becomes higher, the spin polarization rate of the injected electrons becomes higher.

[0042] Hereinafter, electrons that are spin-polarized will be referred to as spin-polarized electrons. The majority spins and the minority spins of spin-polarized electrons are in parallel with the majority spins and the minority spins of the ferromagnetic source 3. The spin-polarized electrons injected to the channel are transported to the Schottky barrier interface of the ferromagnetic drain 5 by virtue of the bias V_{DS}, while being attracted toward the interface between the gate insulating film and the semiconductor by virtue of the bias V_{GS}. In the case where the ferromagnetic source 3 and the ferromagnetic drain 5 exhibit a parallel magnetization configuration, the majority spins and the minority spins of spin-polarized electrons are in parallel with the majority spins and the minority spins of the ferromagnetic drain 5. Accordingly, the spin-polarized electrons injected to the ferromagnetic drain 5 pass through the ferromagnetic drain 5, and become a current flowing into the ferromagnetic drain (hereinafter, the current will be referred to as "drain current"), without adverse influence of spin-dependent diffusion. Particularly, in the case where the ferromagnetic source 3 and the ferromagnetic drain 5 are in a parallel magnetization configuration, the bias V_{GS} of a predetermined drain current is set as a threshold voltage V_T.

[0043] On the other hand, in a case where the ferromagnetic source 3 and the ferromagnetic drain 5 are in an antiparallel magnetization configuration, the majority spins among spin-polarized electrons injected to the channel are in antiparallel with the majority spins of the ferromagnetic drain 5 (see Fig. 4D). Accordingly, the spin-polarized electrons of the channel cause electric resistance due to spin-dependent scattering in the ferromagnetic drain 5. Therefore, even if the MISFET has a uniform bias, the drain current becomes smaller due to the spin-dependent scattering in the antiparallel magnetization configuration, compared with the case of parallel magnetization. In short, the transmission (mutual) conductance in the case where the relative magnetization between the ferromagnetic source 3 and the ferromagnetic drain 5 is in an antiparallel state is smaller than that in the case where the relative magnetization is in a parallel state. If the channel length is equal to or shorter than the mean free path with respect to the carrier energy relaxation, the carriers in the channel are conducted in a ballistic manner. Therefore, a magnetoresistive effect that is similar to a tunneling magnetoresistive effect can be expected. In such a case, the variation in tarns-conductance becomes even wider between the parallel magnetization and the antiparallel magnetization.

[0044] Figs. 5A through 5D illustrate the principles of the operation of an inversion n-channel MISFET having the ferromagnetic source 3 and the ferromagnetic drain 5. When the bias V_{DS} (>0) is applied in a parallel magnetization configuration (see Fig. 5A), with the bias V_{GS} being 0, the ferromagnetic source 3 is forward-biased as shown in Fig. 5B, and the ferromagnetic drain 5 is reverse-biased. Since the channel region is of p type, a current is generated when holes are injected from the ferromagnetic drain 5. However, few holes are injected due to the reverse-biased Schottky junction of the ferromagnetic drain 5. Although a low current of a size almost equal to the reverse saturation current of the Schottky junction formed by the holes thermally beyond ϕ_p is generated, this current can be sufficiently reduced by properly adjusting ϕ_p. Accordingly, the MISFET is put into a shut-off state, with the bias V_{GS} being 0.

[0045] When a bias V_{GS} (>V_T) greater than a certain threshold voltage V_T determined from the device structure is applied to the gate electrode 7 (shown in Fig. 1), electrons are induced at the interface between the gate insulating film and the semiconductor, thereby forming an inversion layer (although the threshold voltage V_T differs between the inversion channel type and the accumulation channel type, the threshold voltage is denoted by V_T in either case, for ease of explanation). At this point, a barrier with a height ϕ_p against the electrons in the inversion layer is formed at each junction interface with the ferromagnetic source 3 and the ferromagnetic drain 5 in the channel region. However, the junction of the ferromagnetic drain 5 and the junction of the ferromagnetic source 3 are biased with the bias V_{DS}, as shown in Fig. 5C.

[0046] As described above, by selecting a sufficiently large height ϕ_p, the height ϕ_n (= E_G-ϕ_p) is made small, and spin-polarized electrons are injected to the channel due to heat radiation from the ferromagnetic source 3. Also, even if the height ϕ_n is not so small as to thermally discharge the carriers from the ferromagnetic source 3, the Schottky barrier on the side of the ferromagnetic source 3 is tunneled to inject spin-polarized electrons from the ferromagnetic source 3 to the channel, as in the case of the accumulation channel type.

[0047] The spin-polarized electrons injected to the channel are transported to the Schottky barrier interface on the side of the ferromagnetic drain 5 by the bias V_{DS}. In the case where the ferromagnetic source 3 and the ferromagnetic drain 5 are in the parallel magnetization configuration, the majority spins and the minority spins of the spin-polarized electrons are in parallel with the majority spins and the minority spins of the ferromagnetic drain 5. Accordingly, in the case of parallel magnetization, the spin-polarized electrons injected to the ferromagnetic drain 5 pass through the ferromagnetic drain 5 and become a drain current, without adverse influence of spin-dependent scattering, as in the case of the accumulation channel type.

[0048] Meanwhile, in the case where the ferromagnetic source 3 and the ferromagnetic drain 5 are in the antiparallel magnetization configuration as shown in Fig. 5D, the majority spins of the spin-polarized electrons injected to the channel are in antiparallel with the majority spins of the ferromagnetic drain 5. Accordingly, the spin-polarized electrons cause electric resistance due to spin-dependent scattering in the ferromagnetic drain 5. In this manner, the tarns-conductance of a MISFET of the inversion channel type also varies depending on the relative magnetization between the ferromagnetic source 3 and the ferromagnetic drain 5. Even with the same bias, the drain current in the case where the ferromagnetic source 3 and the ferromagnetic drain 5 are in an antiparallel magnetization configuration becomes lower than that in the case of parallel magnetization. Also, if the channel length is equal to or shorter than the mean free path with respect to the carrier energy relaxation, a magnetoresistive effect that is similar to a tunneling magnetoresistive effect can be expected. In such a case, the variation in tarns-conductance becomes even wider between the parallel magnetization and the antiparallel magnetization.

[0049] Next, a case where a half metal is used as a ferromagnetic body is described. Referring to Figs. 6A through 6D, the principles of the operation of a MISFET of the accumulation n-channel type in the case where a half metal is used for the ferromagnetic source and the ferromagnetic drain are described. Fig. 6A shows the energy band structure in a parallel magnetization configuration, and corresponds to Fig. 3A.

[0050] Fig. 6B shows the potential shape in a case where a bias V_{DS} (>0) is applied, with a bias V_{GS} being 0. Hereinafter, the spins belonging to the metallic spins band of the ferromagnetic source 3a will be referred to as "up spins", while the spins belonging to the semiconductor spins band will be referred to as "down spins". For the up spins belonging to the metallic spin band, a Schottky junction with a height of ϕ_n is formed at the junction interface with the semiconductor layer 1, and the bias V_{DS} is divided between the source-side Schottky junction and the drain-side Schottky junction. Accordingly, the Schottky junction of the ferromagnetic drain 5a is forward-biased, while the Schottky junction of the ferromagnetic source 3a is reverse-biased. At this point, the bias V_{DS} is applied in such a manner that the Fermi energy E_F of the ferromagnetic source 3a crosses the band edge of the source-side Schottky barrier, but the barrier width d of the Schottky junction is made so thick that the up spins are not tunneled from the metallic spin band of the ferromagnetic source 3a. With the V_{GS} being 0, tunnel injection of the up spins in the metallic spin band of the ferromagnetic source 3a is restricted in the channel region. Also, the up spins can be injected as a reverse saturation current of the Schottky junction caused by holes thermally beyond the barrier height ϕ_n of the Schottky junction. However, the current can be made sufficiently lower by properly adjusting the value of ϕ_n.

[0051] Meanwhile, the band gap of the semiconductor spin band of the ferromagnetic source 3a having down spins forms an energy barrier with a height ϕ_n' between the semiconductor spins band of the ferromagnetic source 3a and the non-magnetic contact 3b. Since no conduction carriers exist in the semiconductor spin band of the ferromagnetic source 3a, the down spins tunnels the semiconductor spin band of the ferromagnetic source 3a from the non-magnetic contact 3b, or thermally go beyond the barrier, so as to inject the down spins to the semiconductor layer 1. The ferromagnetic source 3a is made sufficiently thick, and the height ϕ_n' of the energy barrier, seen from the non-magnetic metal electrode 3b, is made sufficiently large, so that the probability of the down spins being injected to the channel region can be made very low, and carriers are not injected. Accordingly, with the bias V_{GS} being 0, a current due to up spins and down spins is hardly generated, and the MISFET is put into a shut-off state.

[0052] When a bias V_{GS} (>0) is applied to the gate electrode 7 (shown in Fig. 1), the electric field in the vicinity of the Schottky barrier on the source side is intensified by the electric flux line directed from the gate electrode 7 to the ferromagnetic source 3a, as shown in Fig. 6C. The width of the Schottky barrier then decreases as shown in Fig. 6C (indicated by d'). Accordingly, the up spins from the metallic spin band of the ferromagnetic source 3a tunnel the Schottky barrier, and are injected to the channel region in the semiconductor layer 1 immediately below the gate insulating film. Here, the down spins from the non-magnetic contact 3b are hardly injected due to the energy barrier with a height ϕ_n' of the semiconductor spin band of the ferromagnetic source 3a. Therefore, the ferromagnetic source 3a made of a half metal selectively injects up spins.

[0053] The up spins injected to the channel are transported to the Schottky barrier interface of the ferromagnetic drain 5a by virtue of the bias V_{DS}. In the case where the ferromagnetic source 3a and the ferromagnetic drain 5a exhibit parallel magnetization, the injected up spins are in parallel with the spins in the metallic spins band of the ferromagnetic drain 5a. Accordingly, the up spins injected to the ferromagnetic drain 5a pass through the ferromagnetic drain 5a, and become a drain current, without adverse influence of spin-dependent diffusion. Particularly, in the case where the ferromagnetic source 3a and the ferromagnetic drain 5a exhibit parallel magnetization, the bias V_{GS} that generates a predetermined drain current is set as a threshold voltage V_T.

[0054] On the other hand, in a case where the ferromagnetic source 3a and the ferromagnetic drain 5a exhibit antiparallel magnetization, the up spins injected to the channel are in antiparallel with the spins in the metallic spin band of the ferromagnetic drain 5a, but are in parallel with the spins in the semiconductor spin band, as shown in Fig. 6D. Accordingly, the up spins injected to the channel sense the ferromagnetic drain 5a as the energy barrier with a height of ΔE_C. The film thickness of the ferromagnetic drain 5a and the height ΔE_C are adjusted so that the up spins in the channel cannot tunnel the barrier or cannot thermally go beyond the barrier. In this manner, the up spins injected from the non-magnetic source electrode 3b can hardly pass through the ferromagnetic drain 5a, and a drain current is hardly generated. Thus, the half metal of the ferromagnetic drain 5a transmits only the spins in parallel with the spins in the metallic spin band, but does not transmit the spins in antiparallel with the spins in the metallic spins band.

[0055] From the ferromagnetic source 3a made of a half metal, spin-polarized electrons with a very high spin polarization rate can be injected to the channel. Also, since the spin selection rate of the ferromagnetic drain 5a made of a half metal is very high, the drain current in the case where the ferromagnetic source 3a and the ferromagnetic drain 5 are in an antiparallel magnetization configuration_is much lower than the drain current in the case of parallel magnetization. Accordingly, using a half metal, the difference can be made very large between the drain current in the case where the relative magnetization state of the ferromagnetic source 3a and the ferromagnetic drain 5a exhibits parallel magnetization, and the drain current in the case of antiparallel magnetization, compared with a case of using a regular ferromagnetic metal.

[0056] Next, Referring to Figs. 7A through 7D, the principles of the operation of a MISFET of the inversion n-channel type in the case where a half metal is used for the ferromagnetic source and the ferromagnetic drain are described. In the following, the spins belonging to the metallic spin band of the ferromagnetic source 3a made of a half metal will be referred to "up spins", while the spins belonging to the semiconductor spin band will be referred to "down spins".

[0057] Fig. 7A shows the energy band structure in a parallel magnetization configuration, and corresponds to Fig. 3B. In a case where a bias V_{DS} is applied, with a bias V_{GS} being 0, a current is generated in the MISFET when holes are injected from the drain side, as the semiconductor layer 1 is a p-type semiconductor. However, the Schottky junction by the metal spin band of the half metal of the ferromagnetic drain 5a is reverse-biased, and hole injection is restricted. Although a current almost the same size as the reverse saturation current of the Schottky junction is generated, it can be made sufficiently lower by properly adjusting ϕ_p.

[0058] Also, hole injection from the drain-side non-magnetic contact 5b is also restricted by the energy barrier ϕ_p' of the semiconductor spin band of the ferromagnetic drain 5a. Thus, the MISFET is put into a shut-off state in the case shown in Fig. 7B.

[0059] When a bias V_{GS} greater than the threshold voltage V_T is applied to the gate electrode 7, electrons are induced at the interface between the gate insulating film and the semiconductor, thereby forming an inversion layer (the threshold voltage V_T differs between the inversion channel type and the accumulation channel type). At this point, a barrier with a height ϕ_n is formed with the metallic spin band made of a half metal at each junction interface between the inversion layer and the ferromagnetic source 3a and the ferromagnetic drain 5a, as shown in Fig. 7C.

[0060] By applying the bias V_{DS}, the junctions of the ferromagnetic drain 5a and the ferromagnetic source 3a are biased as shown in Fig. 7C. By selecting a sufficiently large height ϕ_p, the height ϕ_n (= E_G-ϕ_p) is made small, and up spins are injected to the channel due to thermal emission from the metallic spin band of the ferromagnetic source 3a. Also, even if the height ϕ_n is not so small as to thermally inject up spins from the ferromagnetic source 3a, the up spins can be tunnel-injected from the metallic spin band of the ferromagnetic source 3a to the channel as in the case of the accumulation channel type. On the other hand, the down spins in the semiconductor spin band of the ferromagnetic source 3a are hardly injected.

[0061] The up spins injected to the channel are transported to the junction interface on the drain side by the bias V_{DS}. In the case where the ferromagnetic source 3a and the ferromagnetic drain 5a exhibit parallel magnetization, the up spins injected to the channel are in parallel with the spins in the metallic spin band of the ferromagnetic drain 5a. Accordingly, in the case of parallel magnetization, the up spins pass through the metallic spin band of the ferromagnetic drain 5 and become a drain current.

[0062] On the other hand, in a case where the ferromagnetic source 3a and the ferromagnetic drain 5a exhibit antiparallel magnetization, the up spins injected to the channel are in antiparallel with the spins in the metallic spin band of the ferromagnetic drain 5a, but are in parallel with the spins in the semiconductor spin band of the ferromagnetic drain 5a, as shown in Fig. 7D. Accordingly, the up spins injected to the channel sense the ferromagnetic drain 5a as the energy barrier with a height of ΔE_C. The film thickness of the ferromagnetic drain 5a and the height ΔE_C are adjusted so that the up spins in the channel cannot tunnel the barrier or cannot thermally go beyond the energy barrier with a height of ΔE_C. In this manner, drain current components are hardly generated.

[0063] As described above, the half metal of the ferromagnetic drain 5a transmits only the spins that are in parallel with the spins in the metallic spin band. Accordingly, the tarns-conductance can be controlled depending on the relative magnetization state between the ferromagnetic source 3a and the ferromagnetic drain 5a. Thus, the drain current in the case where the ferromagnetic source 3a and the ferromagnetic drain 5a exhibit antiparallel magnetization is lower than that in the case of parallel magnetization.

[0064] In the above described MISFET that has a ferromagnetic source (3 or 3a) and a ferromagnetic drain 5 (5 or 5a) made of a ferromagnetic metal or a half metal, the semiconductor layer 1 may be replaced with an undoped semiconductor or an intrinsic semiconductor. In such a case, the barrier structure formed with the junctions caused between the ferromagnetic metal and the semiconductor differs from a Schottky barrier, but the same MISFET operation can be expected with this barrier structure. In this MISFET, the channel region is formed with an intrinsic semiconductor. Accordingly, adverse influence of impurity scattering is not seen in the channel region, and higher mobility of conduction carriers can be expected. Particularly, in a MISFET with a nanoscale short channel, ballistic conduction of carriers that are effective for high-speed operations can be expected. Also in this MISFET, a variation in threshold voltage is not basically caused, even in a case where scale-downed MISFETs with small threshold voltages are highly integrated. Furthermore, a channel formed with an intrinsic semiconductor is suitable for a SOI structure. Accordingly, with an intrinsic semiconductor used for a channel region, the performance of the MISFET of the present invention and the performance of a non-volatile memory (described later) in which the MISFET is employed can be further increased.

[0065] Next, a MISFET in accordance with a third embodiment of the present invention is described in conjunction with the accompanying drawings. In a MISFET in accordance with this embodiment, the ferromagnetic source and the ferromagnetic drain form Schottky junctions with a semiconductor layer and a thin metal layer with a height desired for a barrier. A ferromagnetic metal or a half metal is formed on the metal layer. Fig. 12 shows an energy band structure of a MISFET in accordance with this embodiment. As shown in Fig. 12, the MISFET in accordance with this embodiment has ferromagnetic metal members 23 and 25 as a source and a drain, and thin metal layers 23a and 25a introduced at the interfaces between a semiconductor layer and the ferromagnetic metal members 23a and 25a. The thin metal layers 23a and 25a are used to control the barrier height. Schottky junctions of the metal layers 23a and 25a and the semiconductor layer 21 with which a desired barrier height ϕ_n can be obtained are first formed, and the ferromagnetic metal layers 23 and 25 are formed on the metal layer 23a and 25a, respectively. The specific example of the materials for the metal layers 23a and 25a include silicides such as $ErSi_x$ or $PtSi_x$, with the Si being the semiconductor layer 21.

[0066] As in the structure shown in Fig. 12, the Schottky barrier height can also be controlled with a structure in which the ferromagnetic metal layers 23 and 25 are replaced with the half metal employed in the second embodiment, or a MISFET having a half-metal ferromagnetic source and a half-metal ferromagnetic drain. Such a structure can also be provided in accordance with the present invention. Alternatively, another semiconductor with which a desired Schottky barrier height at the interface with the ferromagnetic metal or the half metal may be inserted at the interface between the semiconductor layer and the ferromagnetic metal or the half metal. To control the Schottky barrier height, a metal/semiconductor heterostructure may also be inserted at the interface between the semiconductor layer and the ferromagnetic metal or the half metal.

[0067] By the above described technique, the material for the ferromagnetic source and the ferromagnetic drain can be arbitrarily selected, regardless of the Schottky height between the semiconductor layer and the ferromagnetic metal or the half metal.

[0068] Next, a MISFET in accordance with an example useful for understanding the present invention is described in conjunction with the accompanying drawings. According to the invention, the ferromagnetic source and the ferromagnetic drain are formed with Schottky junctions of a ferromagnetic half metal. The MISFET in accordance with this example, on the other hand, has a ferromagnetic source and a ferromagnetic drain made of ferromagnetic semiconductors. With this structure, the same effects as those of the MISFETs of the first through third embodiments can be expected, without Schottky junctions.

[0069] As shown in Fig. 13A, for example, the MISFET has an intrinsic semiconductor 31 used as a channel region, and also has a gate insulator 41 and a gate (electrode) 37 stacked on the intrinsic semiconductor 31. In this MISFET, n-type ferromagnetic semiconductors are used for a ferromagnetic source 33 and a ferromagnetic drain 35, so as to form an n-channel MISFET that can exhibit the same characteristics as those of any of the MISFETs (the MISFET shown in Fig. 2A, for example). To produce a p-channel MISFET, p-channel ferromagnetic semiconductors should be used for the ferromagnetic source and the ferromagnetic drain.

[0070] Next, a MISFET in accordance with another example useful for understanding the present invention is described in conjunction with the accompanying drawings. The MISFET in accordance with this embodiment has a ferromagnetic source and a ferromagnetic drain formed with pn junctions between a semiconductor and ferromagnetic semiconductors (in this case, the MISFET operates as an inversion channel type). As shown in Fig. 13B, for example, n-type ferromagnetic semiconductors are used for a source 53 and a drain 55, and a p-type semiconductor is used for a semiconductor layer 51 that includes the channel region. In this structure, a gate insulating film 61 and a gate (electrode) 57 are also stacked on the p-type semiconductor layer 51. Likewise, p-type ferromagnetic semiconductors may be used for the source and the drain, while an n-type semiconductor is used for the channel region.

[0071] As described in the previous two examples, even when the ferromagnetic source and the ferromagnetic drain are formed with ferromagnetic semiconductors, the drain current differs between parallel magnetization and antiparallel magnetization, due to the spin-dependent scattering at the drain. Also, if the channel length is shorter than the mean free path with respect to the carrier energy relaxation, spin-dependent conduction that is similar to a tunneling magnetoresistive effect can be obtained from the ballistic conduction of the carriers. In such a case, the variation in tarns-conductance between parallel magnetization and antiparallel magnetization can be made wider.

[0072] Examples of the ferromagnetic semiconductors used for the MISFETs from the previous two examples include those with transition metal elements or rare-metal elements such as Mn and Cr incorporated into semiconductors of Si, Ge, Si_xFe_{1-x}, or SiC.

[0073] Next, examples of output characteristics of the MISFETs in accordance with the above described embodiments are described. Fig. 8 shows the V_{DS} dependence of a drain current I_D, with V_{GS} being a parameter. Whether a ferromagnetic metal or a half metal is used for the ferromagnetic source 3 and the ferromagnetic drain 5 in the MISFET in accordance with this embodiment, and whether the MISFET is of the inversion channel type or the accumulation channel type, the MISFET is put into a shutoff state when a voltage equal to or lower than a predetermined threshold voltage V_T determined from the device structure is applied to the gate electrode 7. The state of the MISFET does not depend on the relative magnetization state between the ferromagnetic source 3 and the ferromagnetic drain 5.

[0074] A voltage V_1 ($>V_T$) equal to or higher than the threshold voltage is applied to the gate electrode 7, so that the transistor can be put into a conductive state. Here, the drain current I_D generated between the ferromagnetic source 3 and the ferromagnetic drain 5 varies depending on the relative magnetization state of the ferromagnetic drain 5 with respect to the ferromagnetic source 3. With the same bias being applied, the drain current I_D is higher ($I_{D\uparrow\uparrow}$ in Fig. 8) in the case of parallel magnetization, and the drain current I_D is lower ($I_{D\uparrow\downarrow}$ in Fig. 8) in the case of antiparallel magnetization. In other words, the transmission (mutual) conductance of the MISFET is controlled by adjusting the magnetization state between the ferromagnetic source 3 and the ferromagnetic drain 5. Accordingly, in the MISFET of this embodiment, the drain current I_D can be controlled by adjusting the voltage to be applied to the gate electrode 7, and the tarns-conductance depends on the relative magnetization state of the ferromagnetic drain 5 with respect to the ferromagnetic source 3.

[0075] A ferromagnetic body can maintain a magnetization direction unless a magnetic field greater than its coercive force is applied from the outside. Accordingly, in the MISFET in accordance with this embodiment, binary information can be stored in accordance with the relative magnetization state between the ferromagnetic source and the ferromagnetic drain to parallel magnetization or antiparallel magnetization.

[0076] In the above described MISFET, the relative magnetization state between the ferromagnetic source and the ferromagnetic drain can be electrically sensed based on the size of the drain current or the tarns-conductance. Accordingly, the above described MISFET alone can form a 1-bit non-volatile memory cell.

[0077] Fig. 9A illustrates an example structure of a memory circuit that employs MISFETs in accordance with this embodiment. In the memory circuit shown in Fig. 9A, MISFETs are arranged in a matrix fashion. In each MISFET, a source terminal S is grounded while a drain terminal D and a gate terminal G are respectively connected to a read bit line BL and a read word line WL. Also, a rewrite word line and a rewrite bit line are arranged to cross each other, while being electrically insulated from the other lines in the MISFET. The read bit line BL and the read word line WL may also serve as the rewrite bit line and the rewrite word line. Fig. 9A shows the cell structure in the case where the read bit line BL and the read word line WL also serve as the rewrite bit line and the rewrite word line. In the example shown in Fig. 9A, each MISFET alone can form a memory cell, and a very simple line arrangement can be employed.

[0078] A conventional MRAM memory cell includes one MTJ, one MISFET, and four lines (see Fig. 10). In this structure, it is difficult to reduce the cell area by sharing a source between adjacent cells, due to the existence of the MTJ and a rewrite word line. On the other hand, a memory cell in accordance with this embodiment has a simplest structure that is formed with one MISFET and three lines, as shown in Fig. 9A. With such memory cells, a layout suitable for a small-sized memory can be readily employed.

[0079] For example, it is possible to form a structure in which one ferromagnetic source is shared between two MISFETs of this embodiment. Fig. 11 is a cross-sectional view of a memory cell with the shared source structure. The memory cell shown in Fig. 11 includes a first MISFET and a second MISFET that are adjacent to each other, a word line WL that connects the gate electrode G1 of the first MISFET and the gate electrode G2 of the second MISFET, a first bit line BL1 that is connected to the first ferromagnetic drain D1 of the first MISFET, a second bit line BL2 that is connected to the second ferromagnetic drain D2 of the second MISFET, a ferromagnetic source S that is shared between the first and second MISFETs, and a line for grounding the ferromagnetic source S. Since the source is shared in this structure, a cell structure that is more suitable for a high-density memory can be formed.

[0080] In the following, the operation of a memory cell is described in conjunction with Fig. 9A. The above described rewrite/read bit line and the rewrite/read word line that are shared are referred to simply as the bit line BL and the word line WL. To rewrite information, the coercive force of the ferromagnetic source 3 or the ferromagnetic drain 5 is changed, of the relative magnetization direction of the ferromagnetic drain 5 with respect to the ferromagnetic source 3 is adjusted to either parallel magnetization or antiparallel magnetization in the MISFET in accordance with this embodiment. For example, parallel magnetization and antiparallel magnetization are represented by the binary information of "0" and "1", respectively. More specifically, a current is applied to the bit line BL and the word line WL that crosses each other on the selected memory cell, and information is stored by inverting the magnetization of the ferromagnetic body with smaller coercive force or the ferromagnetic body without a fixed magnetization direction of the memory cell selected by a compound magnetic field induced by the current flowing through the respective lines. Here, the value of the current to be applied to the respective lines should be determined so as not to cause magnetization inversion with a magnetic field induced only from one of the lines. Thus, the unselected cells connected to the bit line BL or the word line WL to which the selected cell is also connected can be protected from magnetization inversion.

[0081] To read information, a voltage is applied to the word line WL connected to the selected cell, so as to energize the MISFET of this embodiment. A drain voltage is then applied to the bit line BL, so as to detect the size of the drain current I_D. In the MISFET in accordance with this embodiment, in the case where the relative magnetization state of the ferromagnetic drain with respect to the ferromagnetic source exhibits parallel magnetization, the tarns-conductance is great, and a high drain current I_D is generated. In the case of antiparallel magnetization, on the other hand, the tarns-conductance is small, and the drain current I_D is low. Based on the size of the drain current I_D, the relative magnetization between the ferromagnetic source and the ferromagnetic drain can be detected. Alternatively, the detection may be carried out by applying a necessary bias through precharging.

[0082] In a regular MTJ, the current in the case of parallel magnetization is generated by the tunneling between the state densities of the majority spins in the two ferromagnetic electrodes, and the tunneling between the state densities of the minority spins in the two ferromagnetic electrodes. In the case of antiparallel magnetization, the current is generated by the tunneling from the state density of the minority spins to the state density of the majority spins, and the tunneling from the state density of the majority spins to the state density of the minority spins. Accordingly, the currents flowing in the case of parallel magnetization and antiparallel magnetization contains current components generated from minority spins. Therefore, it is not easy to increase the ratio of the current in the case of parallel magnetization to the current in the case of antiparallel magnetization.

[0083] In the MISFET having the ferromagnetic source and the ferromagnetic drain made of a half metal in accordance with this embodiment, on the other hand, only the spins belonging to the metallic spin band in the ferromagnetic source can be injected to the channel, due to the junction between the half metal and the semiconductor layer. Further, only the spins in parallel with the spins belonging to the metallic spin band in the ferromagnetic drain can be extracted and used as a drain current (hereinafter, this effect of a half metal will be referred to as the "spin filter effect").

[0084] In the MISFET having the ferromagnetic source and the ferromagnetic drain made of a half metal in accordance with this embodiment, the current ratio (the drain current ratio) between parallel magnetization and antiparallel magnetization can be made higher than the current ratio that is obtained in a MTJ. Accordingly, with the MISFET in accordance with this embodiment, a magnetization state can be readily detected in the above described memory circuit.

[0085] Also, in the case where the ferromagnetic source and the ferromagnetic drain are made of a ferromagnetic metal, the spin polarization rate (the spin injection rate) of the carriers injected from the ferromagnetic source can be made higher than the spin polarization rate of the ferromagnetic metal by virtue of a strong field effect that is generated at the source-side Schottky barrier due to the gate bias. With such a strong field effect, the drain current ratio between parallel magnetization and antiparallel magnetization can be made higher than the current ratio in a MTJ.

[0086] With a conventional MTJ, there also has been the problem that the TMR ratio greatly decreases with a bias necessary in the circuit, as the TMR ratio rapidly drops with a decrease in bias voltage. In the MISFET in accordance with this embodiment, on the other hand, the spin-dependent scattering due to the ferromagnetic metal, or the spin filter effect due to the half metal is utilized. Therefore, the bias dependence that is seen in a conventional MTJ is not observed. Accordingly, a high drain current ratio can be achieved with a bias necessary for the circuit.

[0087] Fig. 9B shows a memory circuit that has an output terminal V_o connected to the bit line end of the memory circuit of Fig. 9A, and is connected to a supply voltage V_{DD} via a load R_L branching from the output terminal V_o. Fig. 9C shows the static characteristics and operating points of the memory cell of Fig. 9B. Here, a net resistance is used as a load, but it is also possible to use an active load formed with a transistor. As shown in Fig. 9C, the gate voltage V_{GS} is applied to the gate electrode of the MISFET at the time of reading information, and the supply voltage V_{DD} is applied to the bit line BL via the load resistance R_L. The operating point determined by the load resistance R_L moves on the load line shown in Fig. 9C, in accordance with the magnetization state between the ferromagnetic source and the ferromagnetic drain. The output signals V_o in the cases of parallel magnetization and antiparallel magnetization can be represented by $V_{o\uparrow\uparrow}$ and $V_{o\uparrow\downarrow}$ shown in Fig. 9C. The absolute values and the ratio ($V_{o\uparrow\uparrow}/Vo_{\uparrow\downarrow}$) of the output signals can be optimized with the external circuit parameters such as R_L and V_{DD}. For example, in a case where the drain current ratio $I_{D\uparrow\uparrow}/I_{D\uparrow\downarrow}$ is small, a large output signal ratio can be obtained by adjusting (reducing, in this case) the inclination of the load line. Thus, the memory circuit of this embodiment is advantageous in that output signals of desired size can be obtained.

[0088] As described so far, a MISFET having a ferromagnetic source and a ferromagnetic drain in accordance with any of the embodiments of the present invention functions as a transistor that can control the drain current by adjusting the gate voltage, and characteristically controls the transmission (mutual) conductance by adjusting the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source. The relative magnetization between the ferromagnetic source and the ferromagnetic drain can be maintained as it is, without energy supply. This feature is referred to as the non-volatile characteristics. Accordingly, binary information can be stored in a non-volatile manner in accordance with the relative magnetization direction_between the ferromagnetic source and the ferromagnetic drain. Furthermore, with the above described transmission characteristics, the relative magnetization direction can be electrically detected. With the MISFET, one transistor alone can form a 1-bit non-volatile memory cell. Accordingly, with a MISFET of the present invention, a non-volatile memory cell can be readily formed. Thus, a more highly-integrated non-volatile memory circuit that can operate at a higher speed can be obtained.

[0089] Although the preferred embodiments of the present invention have been described, the present invention is not limited to those specific examples. It should be obvious to those skilled in the art that various changes and modifications can be made to the above described embodiments. For instance, any MISFET described in this specification can of course be applied to any memory device or memory circuit described in this specification.

INDUSTRIAL APPLICABILITY

[0090] In a MISFET of the present invention that has a ferromagnetic source and a ferromagnetic drain formed with Schottky junctions made of a ferromagnetic half metal, binary information can be stored in accordance with the relative magnetization direction of the ferromagnetic drain with respect to the ferromagnetic source, and the relative magnetization direction can be electrically detected. Accordingly, with such a MISFET, a single transistor alone can form a non-volatile memory cell. Thus, a high-speed, highly integrated non-volatile memory circuit can be realized.

Claims

1. A transistor using spin-polarized conduction carriers comprising:

a ferromagnetic source (3a) made of a half metal , such as a Heusler alloy like Co_2MnSi, zinc-blende CrAs, CrSb and MnAs, exhibiting a metallic band structure for one of the spins , called metallic spin band, while exhibiting a semiconductor-like or insulator-like band structure for the other spin , called semiconductor spin band, the half metal being a ferromagnetic body, configured such that in operation spin-polarized

conduction carriers are injected from the ferromagnetic source;
a ferromagnetic drain (5a) made of a half metal and configured such that in operation it receives the spin-polarized conduction carriers injected from the ferromagnetic source (3a); and
a semiconductor layer (1) that is provided between the ferromagnetic source (3a) and the ferromagnetic drain (5a), and is joined to the ferromagnetic source (3a) and the ferromagnetic drain (5a);
a gate electrode (7) associated with the semiconductor layer (1); and
contacts (3b, 5b) made of a non-magnetic metal or a non-magnetic conductor contacting the ferromagnetic source (3a) and the ferromagnetic drain (5a), wherein
the ferromagnetic source (3a) and the ferromagnetic drain (5a) form Schottky junctions having a Schottky barrier at the interface between the semiconductor layer (1) and the metallic spin band in the respective half metal;
and wherein, the Fermi energy of the non-magnetic contacts (3b, 5b) is at an energy level that falls within the band gap of the semiconductor spin band of the ferromagnetic source (3a) and the ferromagnetic drain (5a).

2. The transistor as claimed in claim 1, further comprising a metal layer (23a, 25a) or another semiconductor layer formed between the ferromagnetic source (3a) and the semiconductor layer (1) and between the ferromagnetic drain (5a) and the semiconductor layer (1).

3. The transistor as claimed in claim 1, wherein the semiconductor layer is an n-type semiconductor layer (1), and a difference between the Fermi energy (E_F) and an energy (E_C^{HM}) of a bottom of a conduction band of the semiconductor spin band is greater than a height (φ_n) of the Schottky barrier formed between the metallic spin band and the semiconductor layer (1).

4. The transistor as claimed in claim 1, wherein the semiconductor layer is a p-type semiconductor layer (1), and a difference between the Fermi energy (E_F) and an energy (E_V^{HM}) of a top of a valence band of the semiconductor spin band is greater than a height (φ_p) of the Schottky barrier formed between the metallic spin band and the semiconductor layer (1).

5. The transistor as claimed in any of claims 1 to 4, wherein the semiconductor spin band of the half metal has a wider band gap than the band gap of the semiconductor layer (1).

6. The transistor as claimed in any of claims 1 to 5, wherein a channel length, that is defined as the length in the carrier conducting direction in the semiconductor layer (1) or the distance between the ferromagnetic source (3a) and the ferromagnetic drain (5a), is so short that the semiconductor layer (1) conducts carriers in a ballistic manner, or the channel length is equal to or shorter than the mean free path associated with carrier energy relaxation.

7. A memory device comprising the transistor as claimed in any of claims 1 to 6,
the transistor arranged to store information in accordance with the relative magnetization direction of the ferromagnetic drain (5a) with respect to the ferromagnetic source (3a),
the information stored in the transistor being detected based on the trans-conductance of the transistor depending on the relative magnetization direction of the ferromagnetic drain (5a) with respect to the ferromagnetic source (3a).

Patentansprüche

1. Transistor, der spinpolarisierte Leitungsträger verwendet, umfassend:

eine ferromagnetische Source (3a), die aus einem Halbmetall, wie einer heuslerschen Legierung wie Co_2, MnSi, Zinkblende-CrAs, CrSb und MnAs, besteht, die eine metallische Bandstruktur für einen der Spins, metallisches Spinband genannt, aufweist, während sie eine halbleiterschichtähnliche oder eine isolatorähnliche Bandstruktur für den anderen Spin,
Halbleiterschicht-Spinband genannt, aufweist, wobei das Halbmetall ein ferromagnetischer Körper ist, der derart konfiguriert ist, dass bei Betrieb spinpolarisierte Leitungsträger von der ferromagnetischen Source eingespeist werden;
ein ferromagnetisches Drain (5a), das aus einem Halbmetall besteht und derart konfiguriert ist, dass es bei Betrieb die spinpolarisierten Leitungsträger empfängt, die von der ferromagnetischen Source (3a) eingespeist werden; und
eine Halbleiterschicht (1), die zwischen der ferromagnetischen Source (3a) und dem ferromagnetischen Drain (5a) bereitgestellt ist und mit der ferromagnetischen Source (3a) und dem ferromagnetischen Drain (5a) verbunden ist;
eine Gate-Elektrode (7), die in Verbindung mit der Halbleiterschicht (1) ist; und
Kontakte (3b, 5b), die aus einem nichtmagnetischen Metall oder einem nichtmagnetischen Leiter bestehen, der die ferromagnetische Source (3a) und das ferromagnetische Drain (5a) berührt, wobei
die ferromagnetische Source (3a) und das fer-

romagnetische Drain (5a) Schottky-Übergänge bilden, die an der Grenzfläche zwischen der Halbleiterschicht (1) und dem metallischen Spinband in dem jeweiligen Halbmetall eine Schottky-Barriere aufweisen;
und wobei die Fermi-Energie der nichtmagnetischen Kontakte (3b, 5b) auf einem Energieniveau ist, das innerhalb der Bandlücke des Halbleiterspinbands der ferromagnetischen Source (3a) und des ferromagnetischen Drains (5a) liegt.

2. Transistor nach Anspruch 1, der ferner eine Metallschicht (23a, 25a) oder andere Halbleiterschicht umfasst, die zwischen der ferromagnetischen Source (3a) und der Halbleiterschicht (1) und zwischen dem ferromagnetischen Drain (5a) und der Halbleiterschicht (1) gebildet ist.

3. Transistor nach Anspruch 1, wobei die Halbleiterschicht eine n-leitende Halbleiterschicht (1) ist und eine Differenz zwischen der Fermi-Energie (E_F) und einer Energie (E_C^{HM}) einer Unterseite eines Leitungsbands des Halbleiter-Spinbands größer als eine Höhe (ϕ_n) der Schottky-Barriere ist, die zwischen dem metallischen Spinband und der Halbleiterschicht (1) gebildet ist.

4. Transistor nach Anspruch 1, wobei die Halbleiterschicht eine p-leitende Halbleiterschicht (1) ist und eine Differenz zwischen der Fermi-Energie (E_F) und einer Energie (E_V^{HM}) einer Oberseite eines Valenzbands des Halbleiter-Spinbands größer als eine Höhe (ϕ_p) der Schottky-Barriere ist, die zwischen dem metallischen Spinband und der Halbleiterschicht (1) gebildet ist.

5. Transistor nach einem der Ansprüche 1 bis 4, wobei das Halbleiter-Spinband des Halbmetalls eine breitere Bandlücke als die Bandlücke der Halbleiterschicht (1) aufweist.

6. Transistor nach einem der Ansprüche 1 bis 5, wobei eine Kanallänge, die als die Länge in der Trägerleitungsrichtung in der Halbleiterschicht (1) oder die Distanz zwischen der ferromagnetischen Source (3a) und dem ferromagnetischen Drain (5a) definiert ist, so kurz ist, dass die Halbleiterschicht (1) Träger in ballistischer Weise leitet, oder die Kanallänge gleich oder kürzer als die mittlere freie Weglänge ist, die mit der Trägerenergierelaxation assoziiert ist.

7. Speichervorrichtung, die den Transistor nach einem der Ansprüche 1 bis 6 umfasst,
wobei der Transistor dafür ausgelegt ist, Informationen gemäß der relativen Magnetisierungsrichtung des ferromagnetischen Drains (5a) in Bezug auf die ferromagnetische Source (3a) zu speichern,
wobei die in dem Transistor gespeicherten Informationen basierend auf der Transkonduktanz des Transistors abhängig von der relativen Magnetisierungsrichtung des ferromagnetischen Drains (5a) in Bezug auf die ferromagnetische Source (3a) erkannt werden.

Revendications

1. Transistor utilisant des supports de conduction à spin polarisé, comprenant :

une source ferromagnétique (3a) constitué d'un demi-métal, comme du Co_2MnSi analogue à un alliage de Heusler, du CrAs mélangé à du zinc, du CrSb et du MnAs,
présenter une structure de bande métallique pour un des spins, appelée bande de spin métallique, tout en présentant une structure de bande analogue à un semi-conducteur ou analogue à un isolant pour l'autre spin, appelée bande de spin à semi-conducteur, le demi-métal étant un corps ferromagnétique configuré de telle sorte qu'en fonctionnement, des supports de conduction à spin polarisé sont injectés à partir de la source ferromagnétique ;
un drain ferromagnétique (5a) constitué d'un demi-métal et configuré de telle sorte qu'en fonctionnement, il reçoit les supports de conduction à spin polarisé injectés à partir de la source ferromagnétique (3a) ; et
une couche semi-conductrice (1) qui est agencée entre la source ferromagnétique (3a) et le drain ferromagnétique (5a), et est reliée à la source ferromagnétique (3a) et au drain ferromagnétique (5a) ;
une électrode de grille (7) associé sa la couche semi-conductrice (1) ; et
des contacts (3b, 5b) constitués d'un métal non magnétique ou d'un conducteur non-magnétique mettant en contact la source ferromagnétique (3a) et le drain ferromagnétique (5a), dans lequel
la source ferromagnétique (3a) et le drain ferromagnétique (5a) forment une jonction Schottky ayant une barrière Schottky au niveau de l'interface entre la couche semi-conductrice (1) et la bande de spin métallique dans le demi-métal respectif ;
et dans lequel l'énergie de Fermi des contacts non-magnétiques (3b, 5b) est à un niveau d'énergie qui tombe dans la largeur de bande interdite de la bande de spin à semi-conducteur de la source ferromagnétique (3a) et du drain ferromagnétique (5a)

2. Transistor selon la revendication 1, comprenant en outre une couche de métal (23a, 25a) ou une autre couche semi-conductrice formé entre la source ferromagnétique (3a) et la couche semi-conductrice (1) et entre le drain ferromagnétique (5a) et la couche semi-conductrice (1).

3. Transistor selon la revendication 1, dans lequel la couche semi-conductrice est une couche semi-conductrice de type n (1), et une différence entre l'énergie de Fermi (E_F) et une énergie ($E_C{}^{HM}$) d'une partie inférieure d'une bande de conduction de la bande de spin à semi-conducteur est supérieure à une hauteur (φ_p) de la barrière Schottky formée entre la bande de spin métallique et la couche semi-conductrice (1).

4. Transistor selon la revendication 1, dans lequel la couche semi-conductrice est une couche semi-conductrice de type p (1), et une différence entre l'énergie de Fermi (EF) et une énergie ($E_V{}^{HM}$) d'une partie supérieure d'une bande de valence de la bande de spin à semi-conducteur est supérieure à une hauteur (φ_p) de la barrière Schottky formée entre la bande de spin métallique et la couche semi-conductrice (1).

5. Transistor selon l'une quelconque des revendications 1 à 4, dans lequel la banque de spin à semi-conducteur du demi-métal a une largeur de bande interdite plus large que la largeur de bande interdite de la couche semi-conductrice (1).

6. Transistor selon l'une quelconque des revendications 1 à 5, dans lequel une longueur de canal, qui est définie comme la longueur dans la direction de conduction de support dans la couche semi-conductrice (1) ou la distance entre la source ferromagnétique (3a) et le drain ferromagnétique (5a) est si courte que la couche semi-conductrice (1) conduit des supports d'une manière balistique, ou la longueur de canal est égale ou plus courte que le trajet libre moyen associé à un relâchement d'énergie de support.

7. Dispositif mémoire comprenant le transistor selon l'une quelconque des revendications 1 à 6, le transistor étant agencé pour stocker des informations selon la direction de polarisation relative du drain ferromagnétique (5a) par rapport à la source ferromagnétique (3a),
les informations stockées dans le transistor étant détectées sur la base de la transconductance du transistor selon la direction de polarisation relative du drain ferromagnétique (5a) par rapport à la source ferromagnétique (3a).

FIG. 1

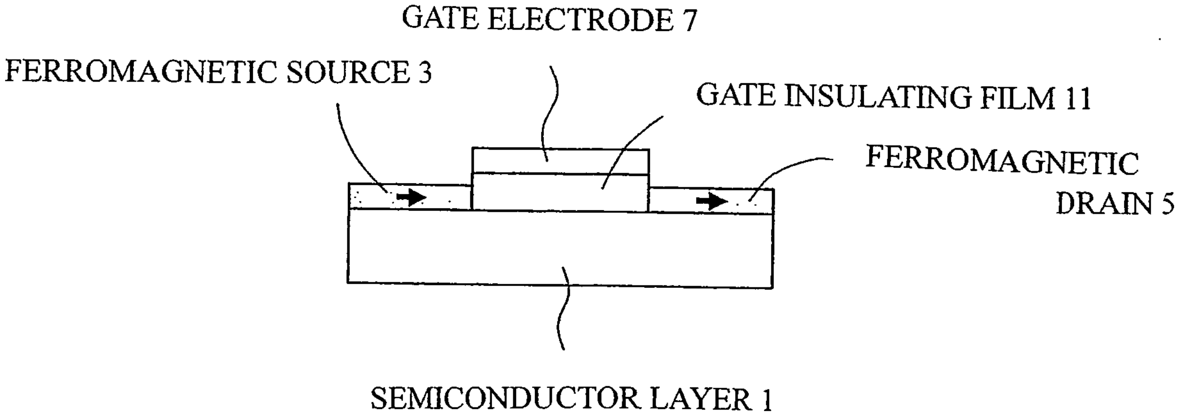

GATE ELECTRODE 7
FERROMAGNETIC SOURCE 3
GATE INSULATING FILM 11
FERROMAGNETIC DRAIN 5
SEMICONDUCTOR LAYER 1

FIG. 2A

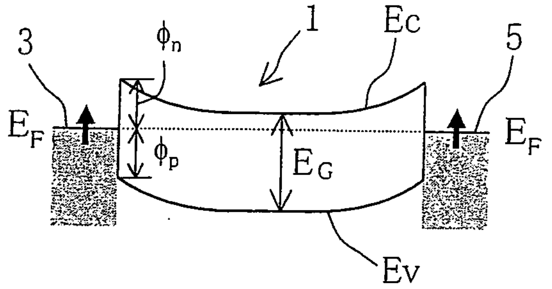


FIG. 2B

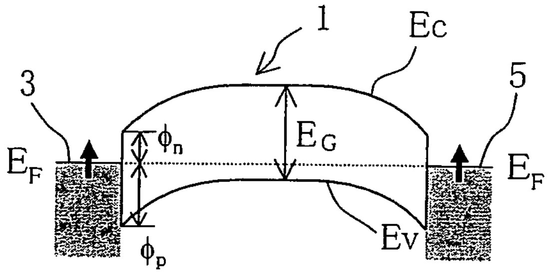


FIG. 3A

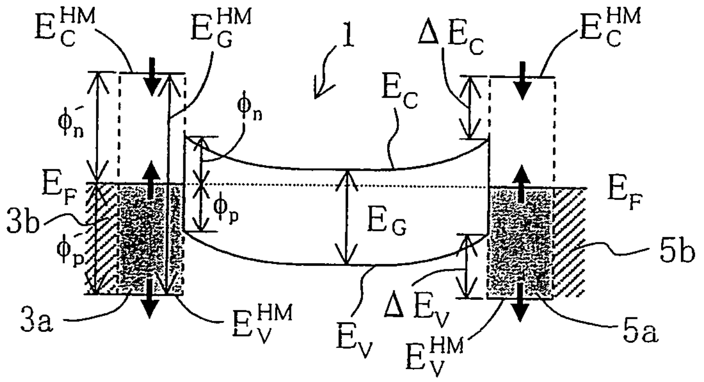


FIG. 3B

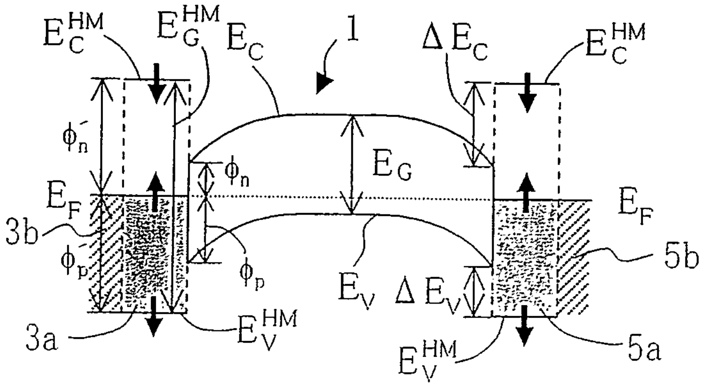


FIG. 4A

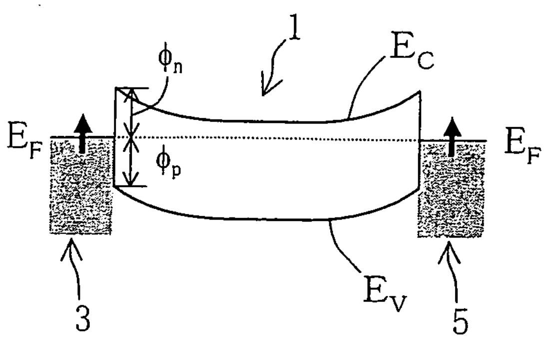


FIG. 4B

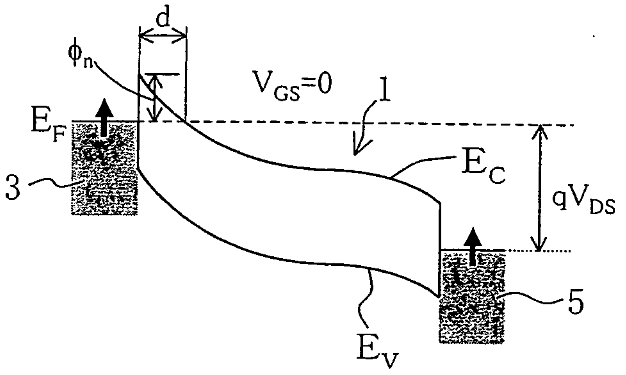


FIG. 4C

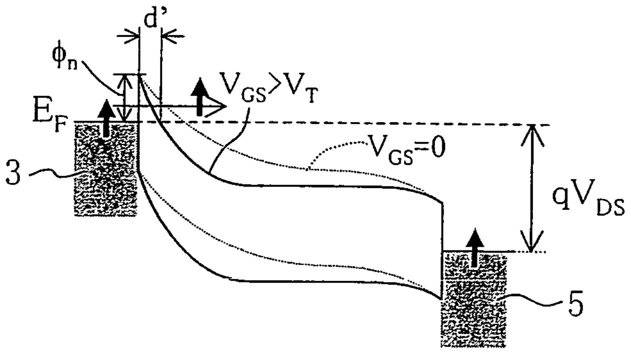


FIG. 4D

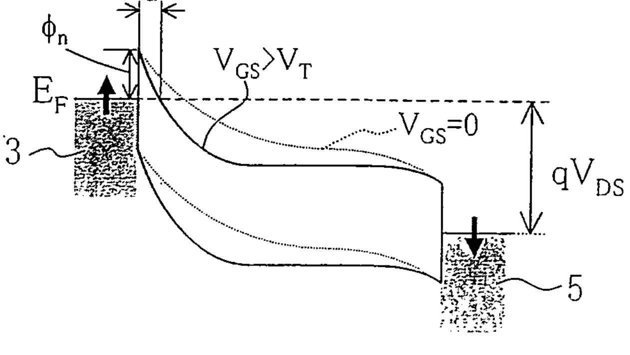


FIG. 5A

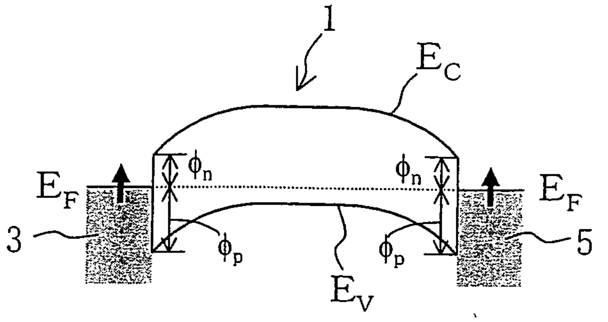


FIG. 5B

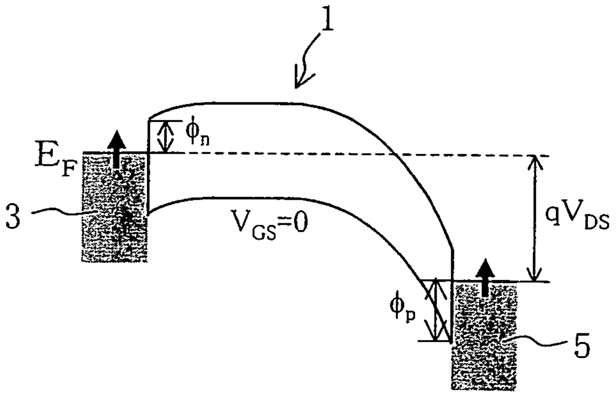


FIG. 5C

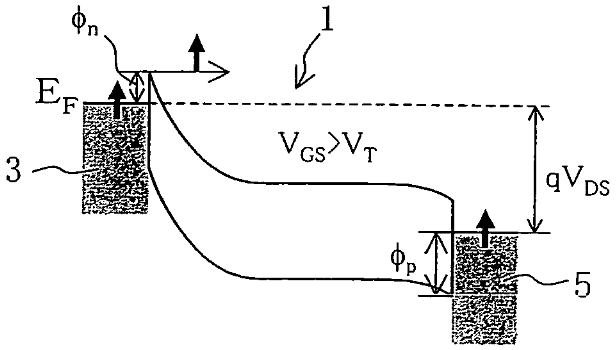


FIG. 5D

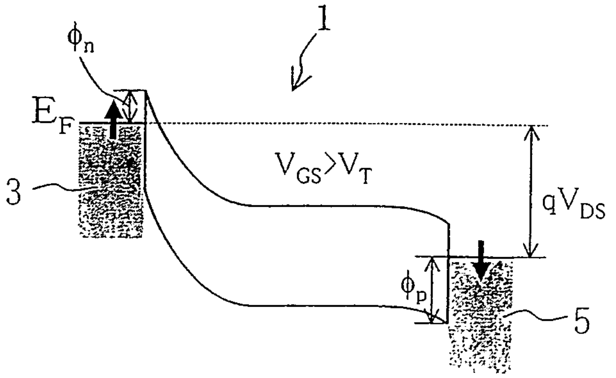


FIG. 6A

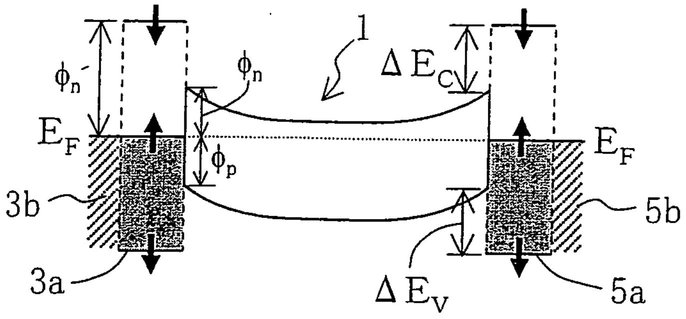


FIG. 6B

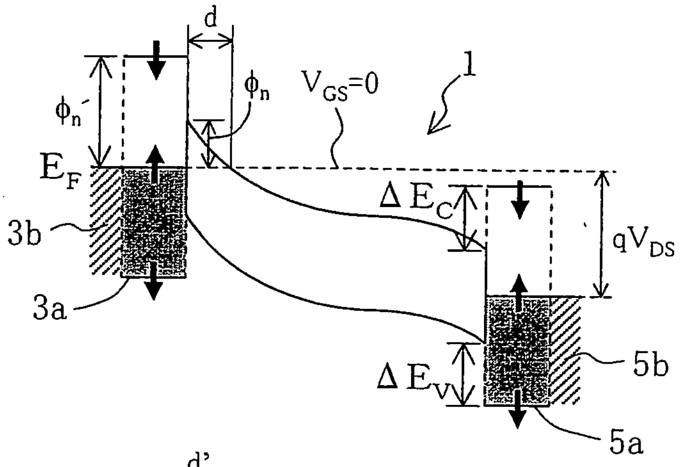


FIG. 6C

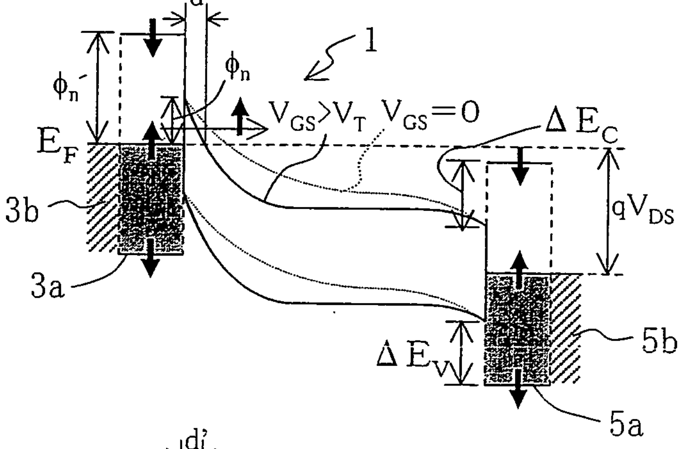


FIG. 6D

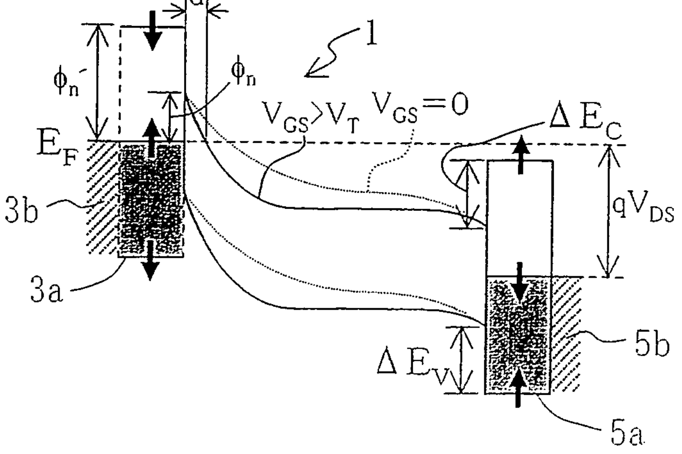


FIG. 7A

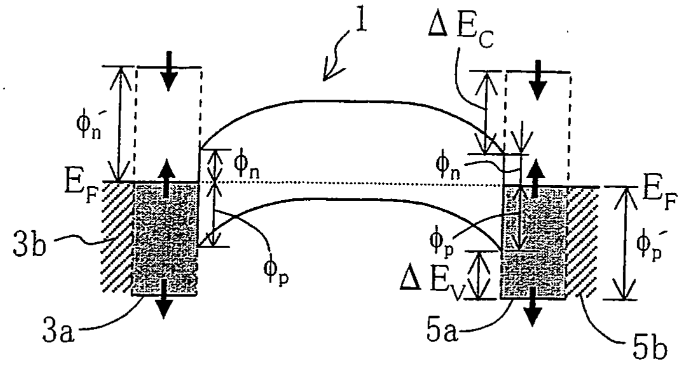


FIG. 7B

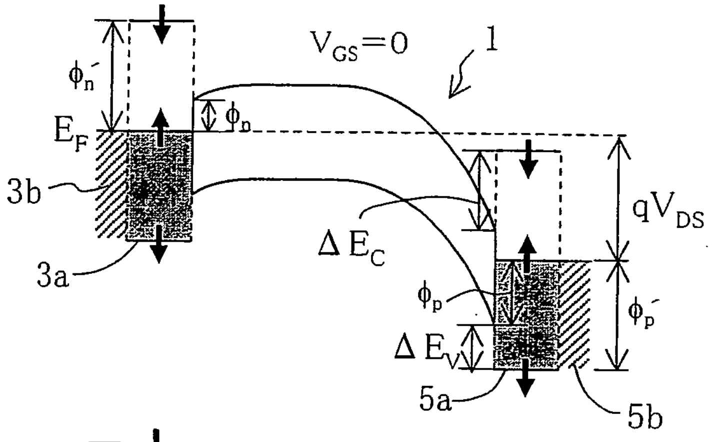


FIG. 7C

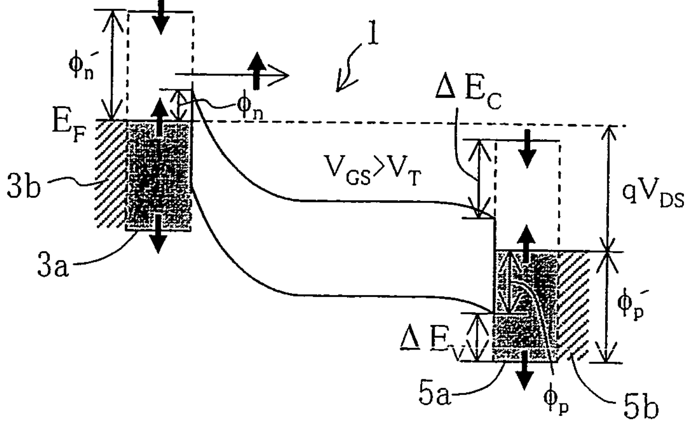


FIG. 7D

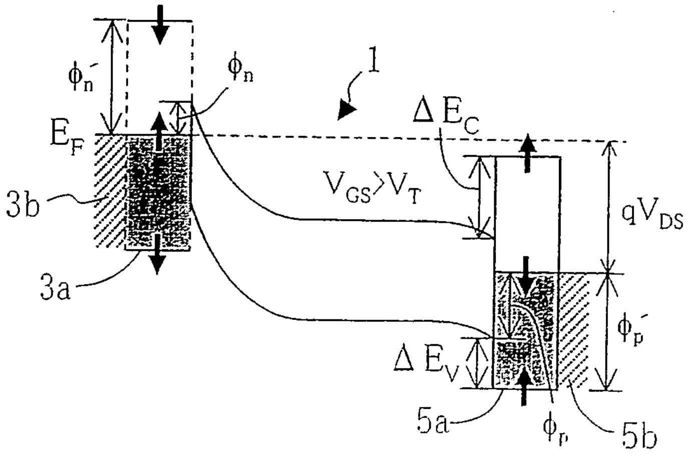


FIG. 8

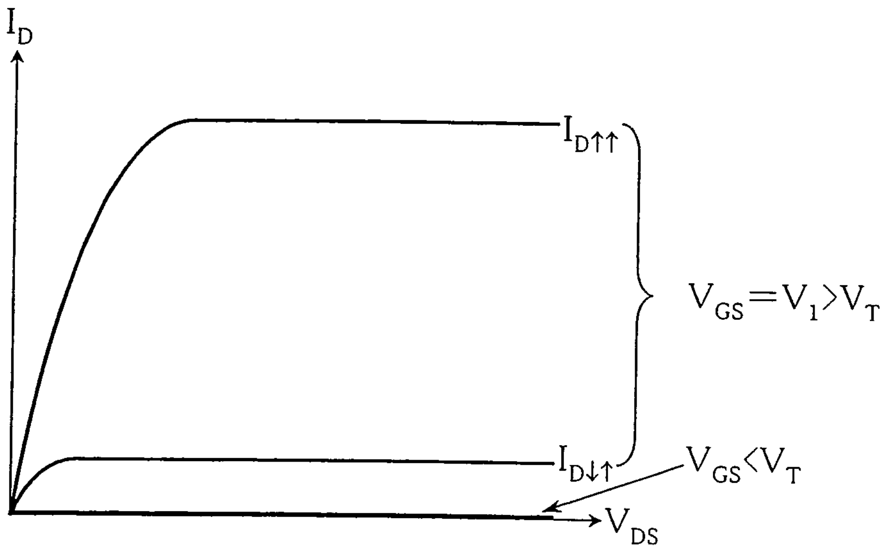

I_D
$I_{D\uparrow\uparrow}$
$V_{GS}=V_1>V_T$
$I_{D\downarrow\uparrow}$
$V_{GS}<V_T$
V_{DS}

FIG. 9A

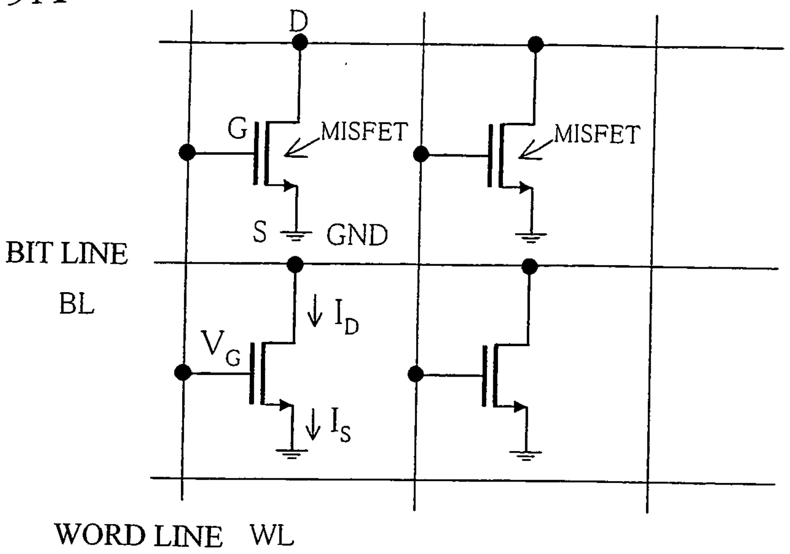


FIG. 9B

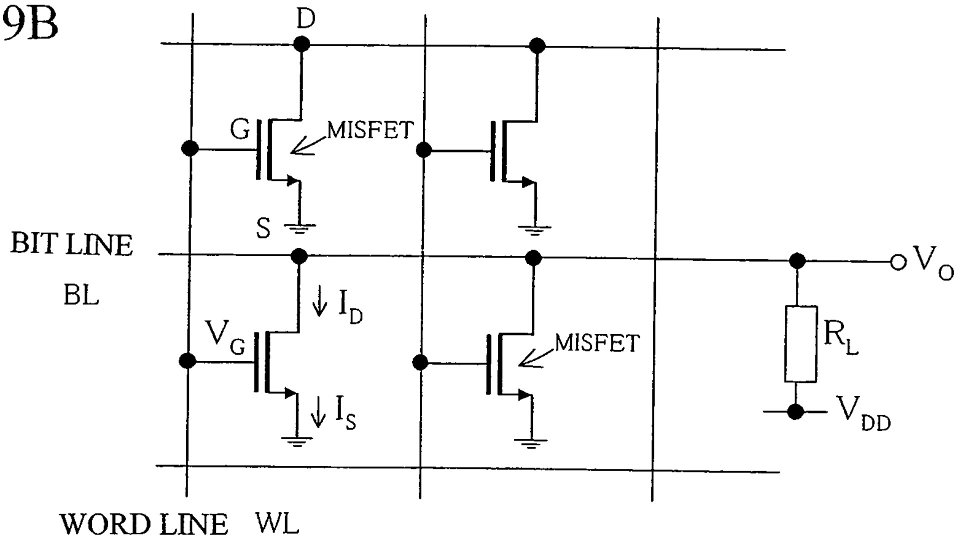


FIG. 9C

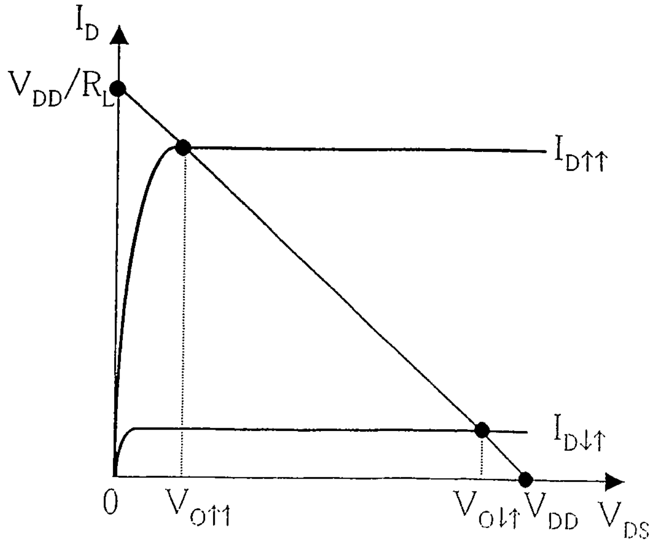


FIG. 10

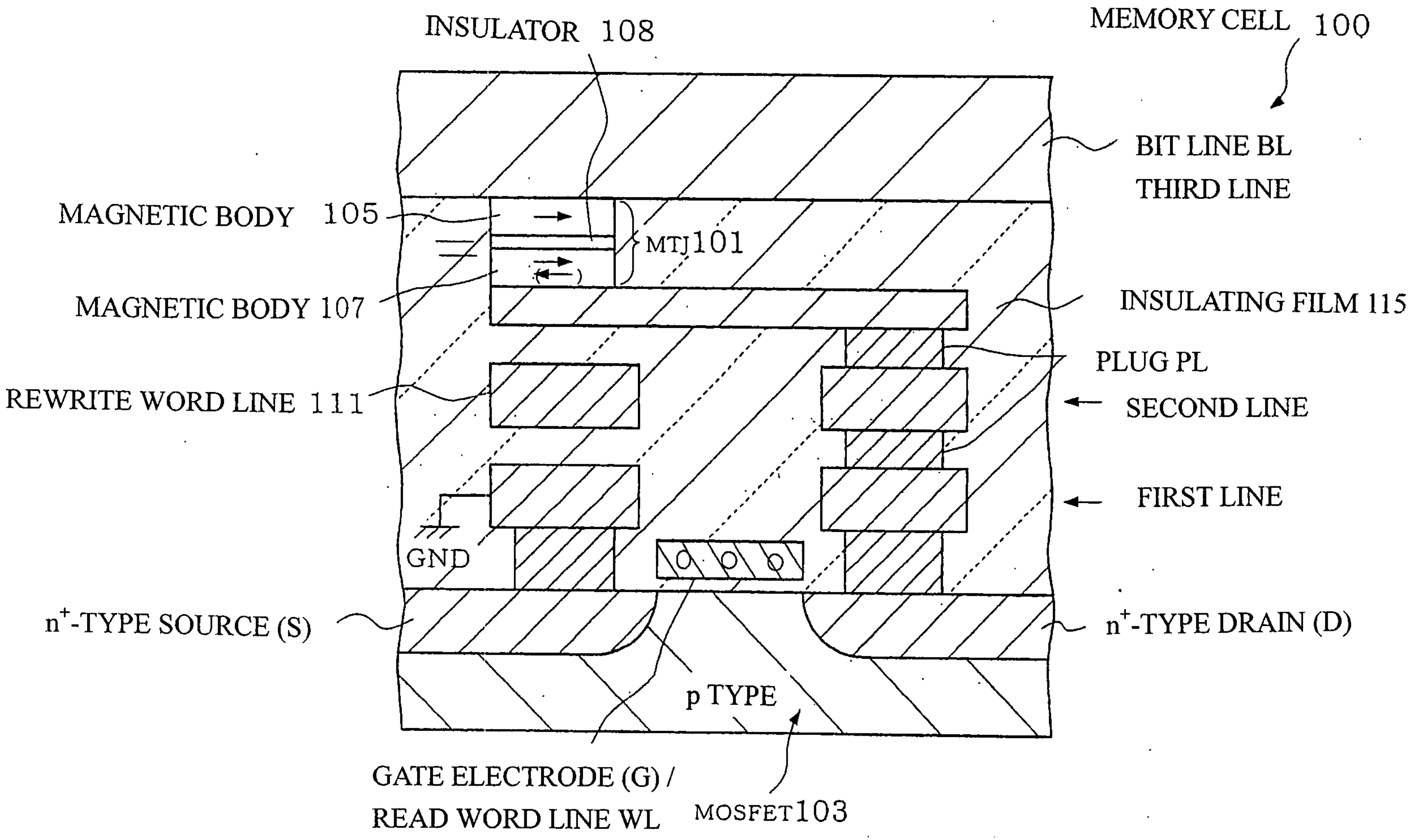

INSULATOR 108
MEMORY CELL 100
BIT LINE BL
THIRD LINE
MAGNETIC BODY 105
MTJ101
MAGNETIC BODY 107
INSULATING FILM 115
PLUG PL
REWRITE WORD LINE 111
SECOND LINE
FIRST LINE
GND
n+-TYPE SOURCE (S)
n+-TYPE DRAIN (D)
p TYPE
GATE ELECTRODE (G) /
READ WORD LINE WL
MOSFET103

FIG. 11

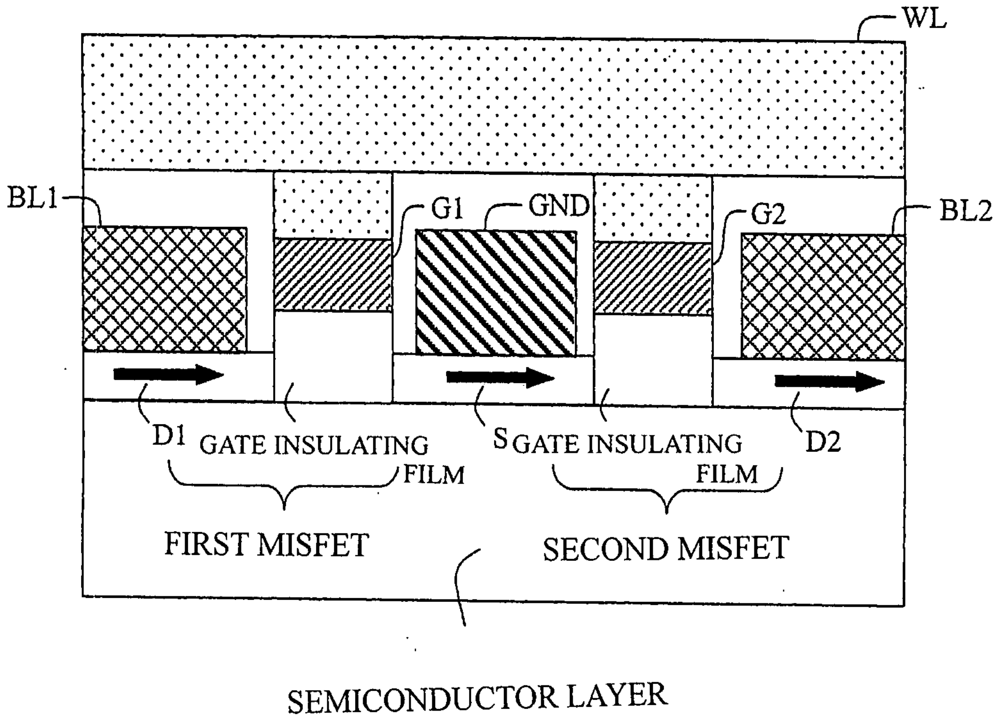

WL
BL1
G1
GND
G2
BL2
D1
GATE INSULATING FILM
S
GATE INSULATING FILM
D2
FIRST MISFET
SECOND MISFET
SEMICONDUCTOR LAYER

FIG. 12

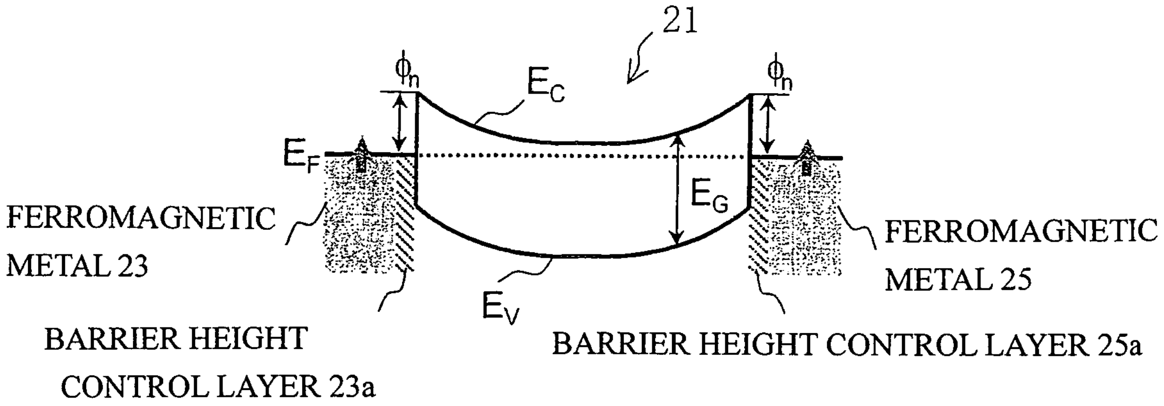


FIG. 13A

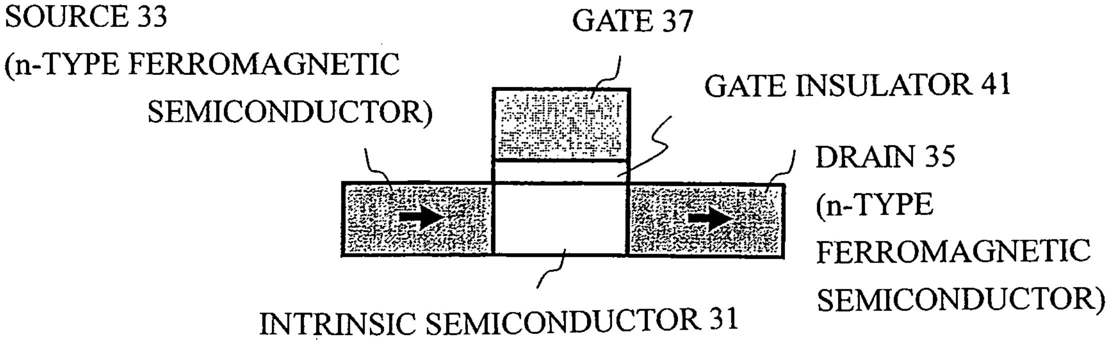
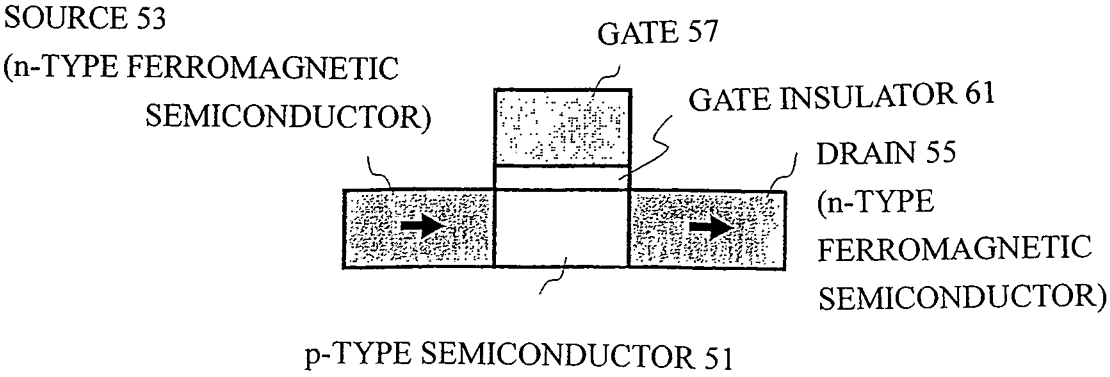


FIG. 13B



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