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Sugahara et al.

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(45) **Date of Patent: May 11, 2010**

(54) **TUNNEL TRANSISTOR HAVING SPIN-DEPENDENT TRANSFER CHARACTERISTICS AND NON-VOLATILE MEMORY USING THE SAME**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 390 days.

(21) Appl. No.: **11/979,346**

(22) Filed: **Nov. 1, 2007**

(65) **Prior Publication Data**

US 2008/0308853 A1 Dec. 18, 2008

Related U.S. Application Data

(62) Division of application No. 10/551,802, filed on Dec. 2, 2005, now Pat. No. 7,397,071.

(51) **Int. Cl.**
H01L 29/70 (2006.01)

(52) **U.S. Cl.** **257/421**; 257/427; 257/E29.323; 438/3; 360/326; 365/157

(58) **Field of Classification Search** 257/421, 257/427, E29.323; 438/3; 365/157; 360/326
See application file for complete search history.

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Assistant Examiner—Jami M Valentine
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(57) **ABSTRACT**

A MISFET the channel region of which is a ferromagnetic semi-conductor has a feature that the drain current can be controlled by the gate voltage and a feature that the transfer conductance can be controlled by the relative directions of magnetization in the ferromagnetic channel region and the ferromagnetic source (or the ferromagnetic drain, or both the ferromagnetic source and ferromagnetic drain). As a result, binary information can be stored in the form of the relative magnetization directions, and the relative magnetization directions are electrically detected. If the magnetism is controlled by the electric field effect of the channel region of a ferromagnetic semiconductor, the current needed to rewrite the information can be greatly reduced. Thus, the MISFET can constitute a high-performance non-volatile memory cell suited to high-density integration.

28 Claims, 18 Drawing Sheets

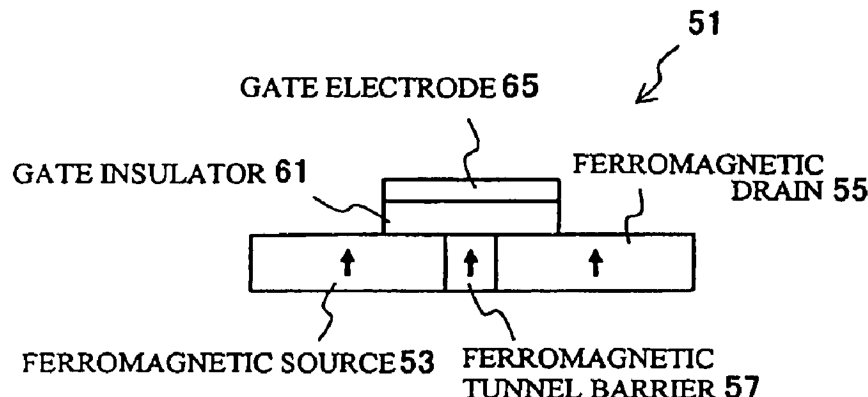

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FIG. 1

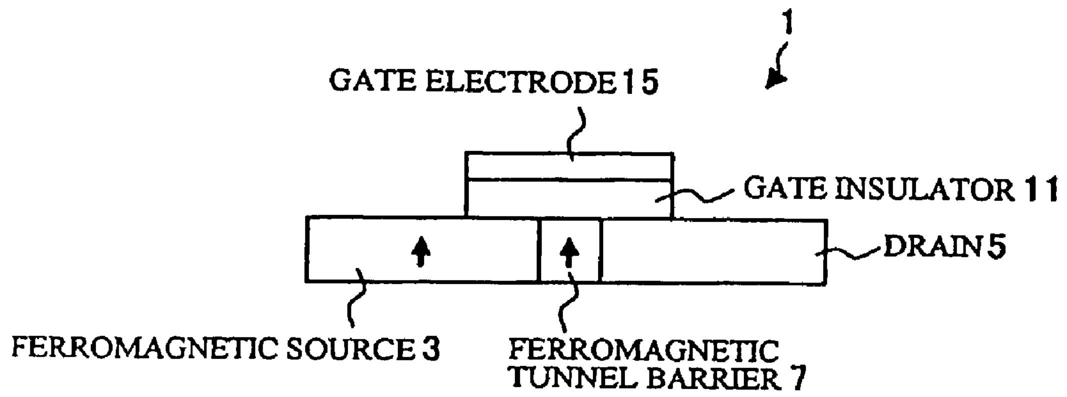


FIG. 2A

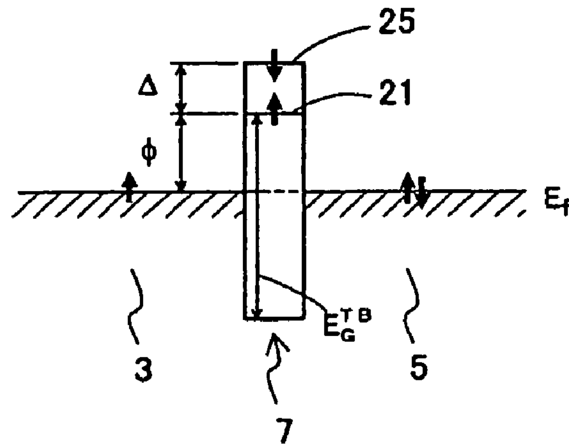


FIG. 2B

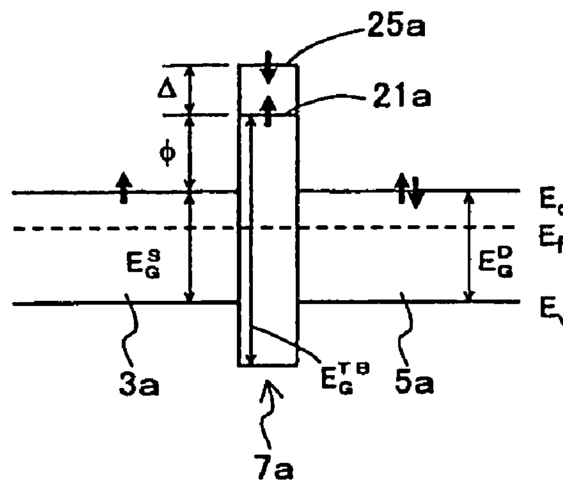


FIG. 2C

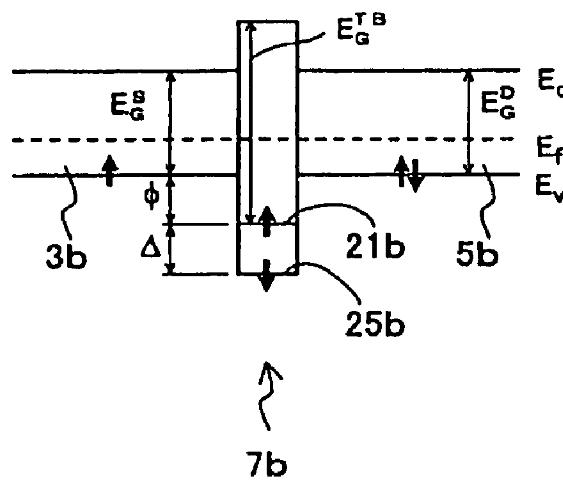


FIG. 3A

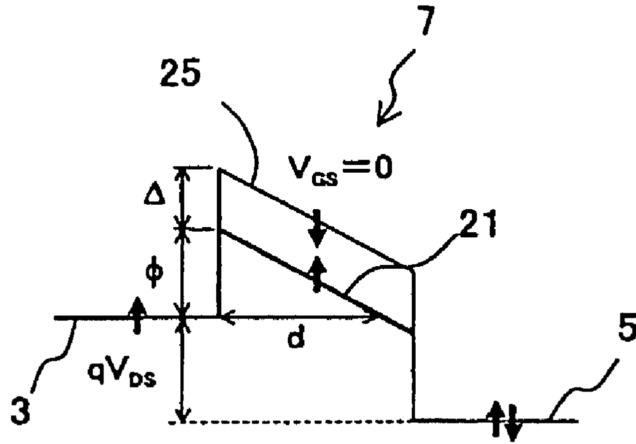


FIG. 3B

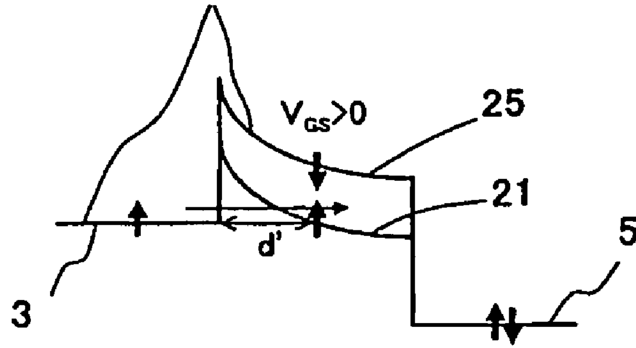


FIG. 3C

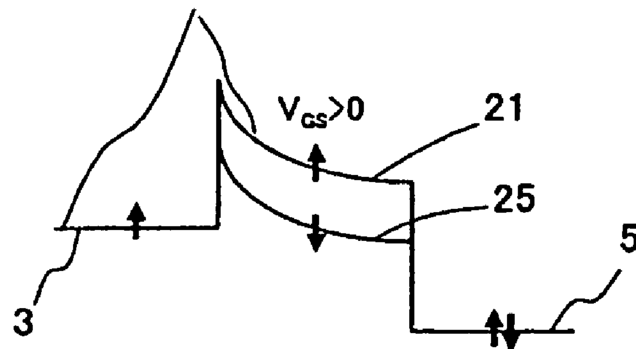


FIG. 4

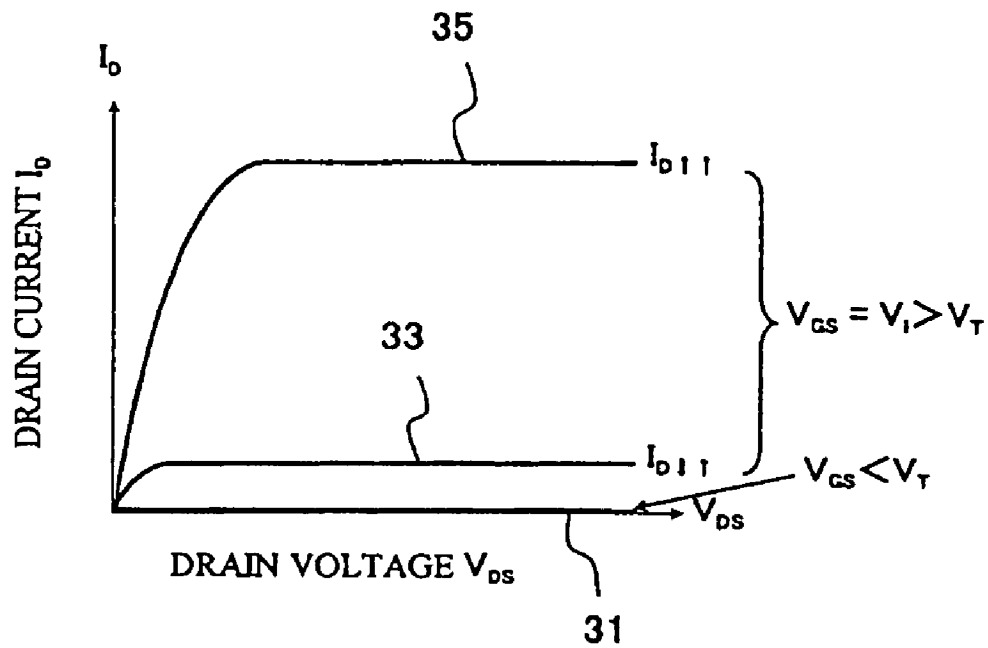


FIG. 5

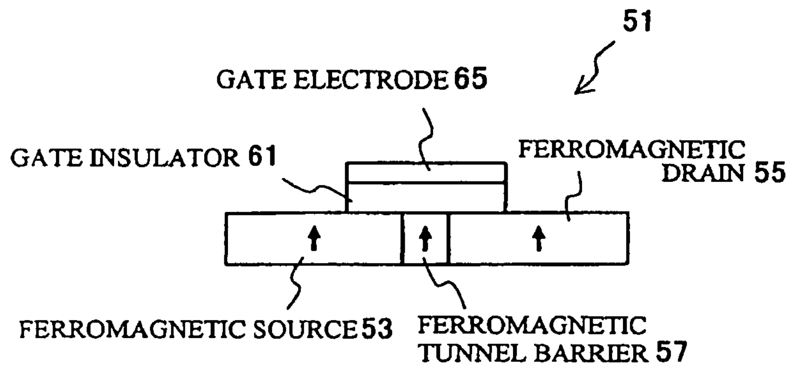


FIG. 6

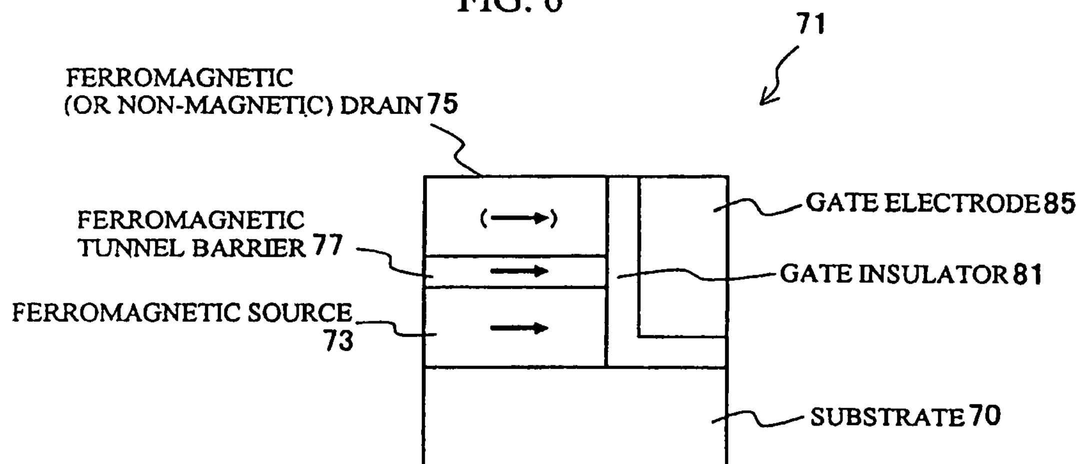


FIG. 7A

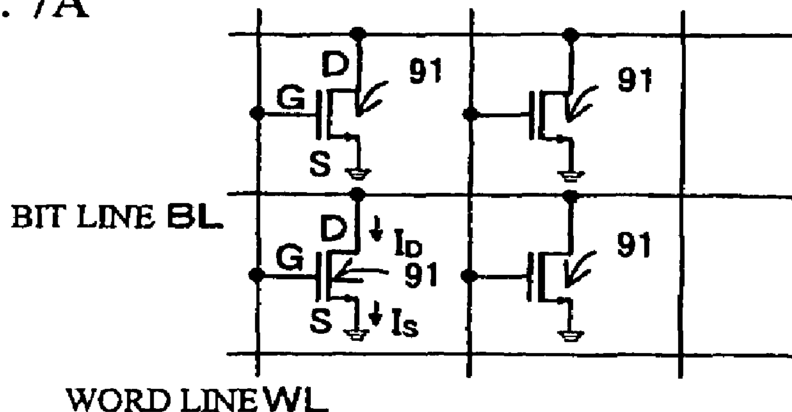


FIG. 7B

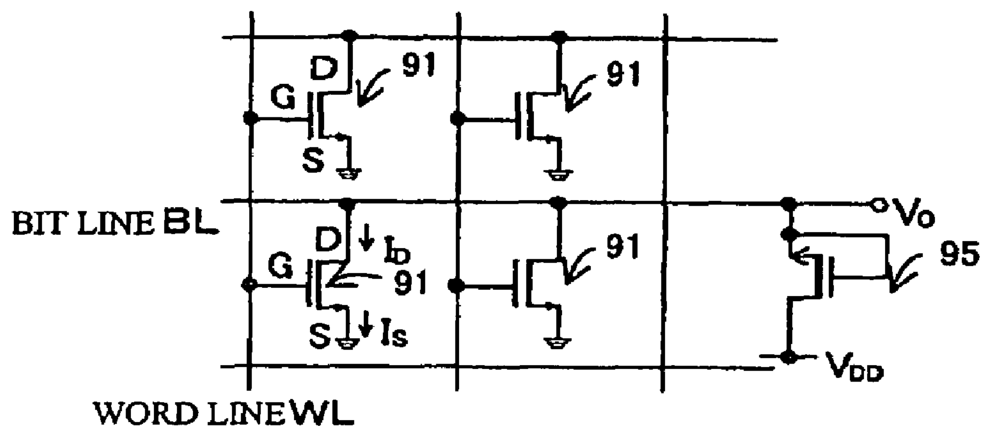
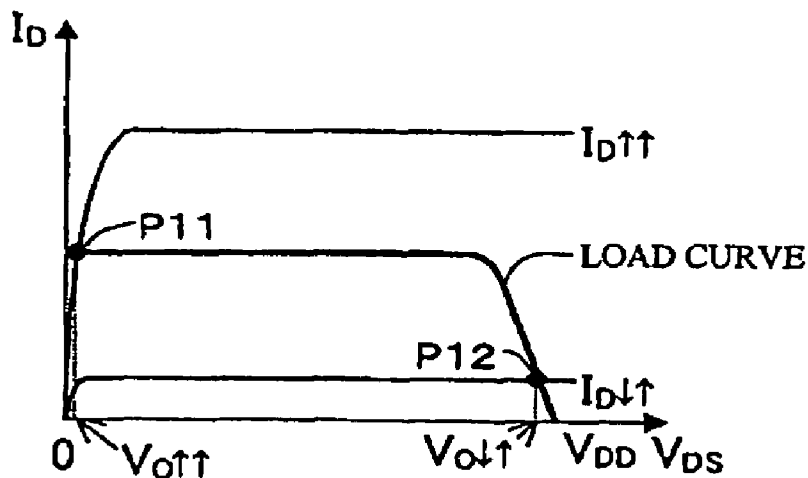


FIG. 7C



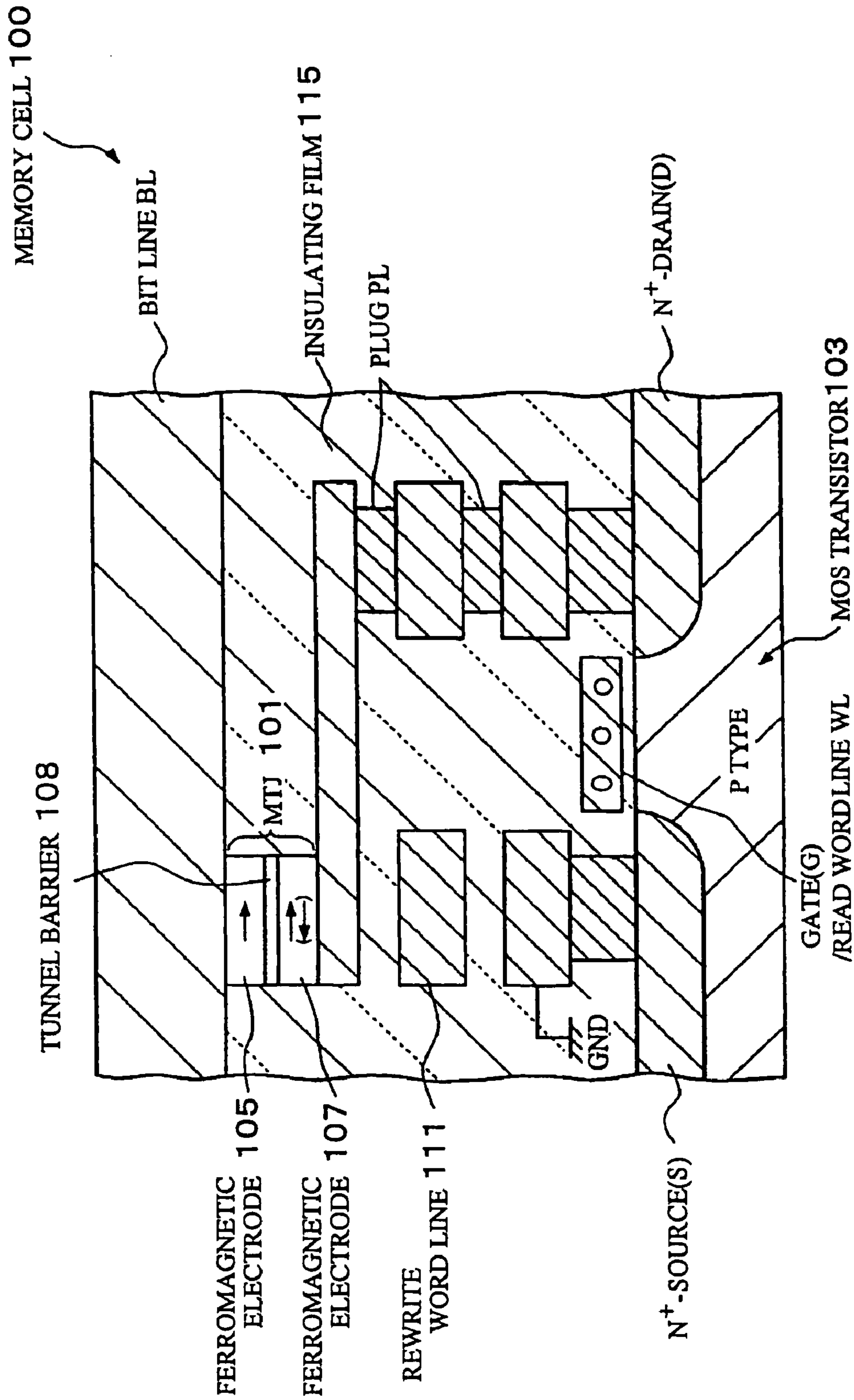


FIG. 8

FIG. 9

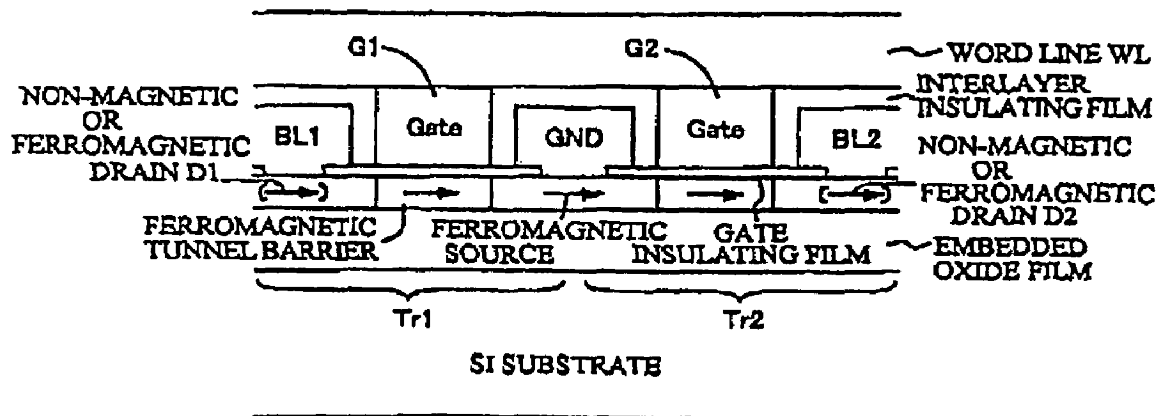


FIG. 10

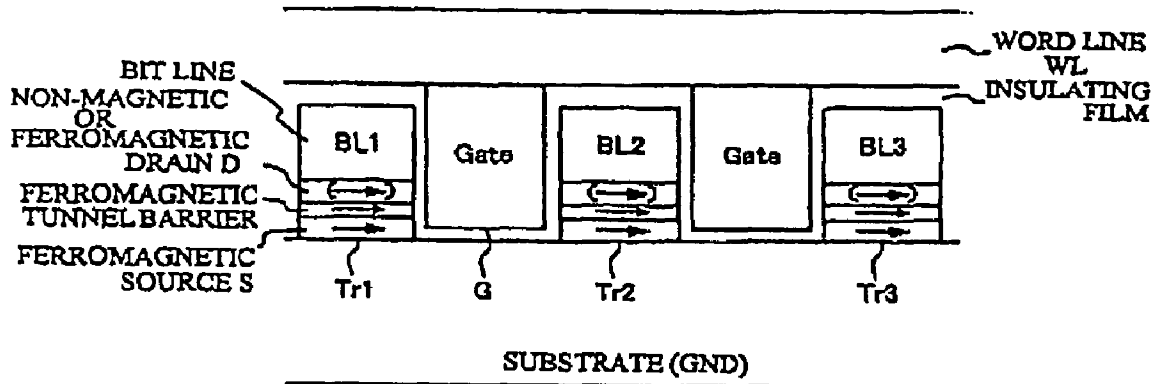
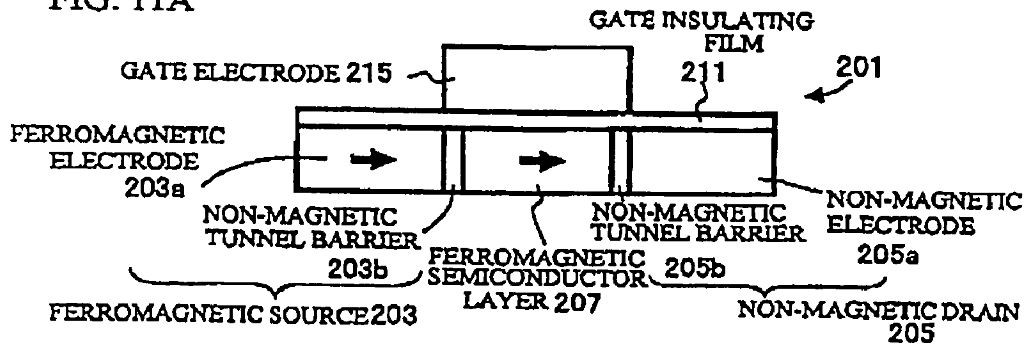


FIG. 11A



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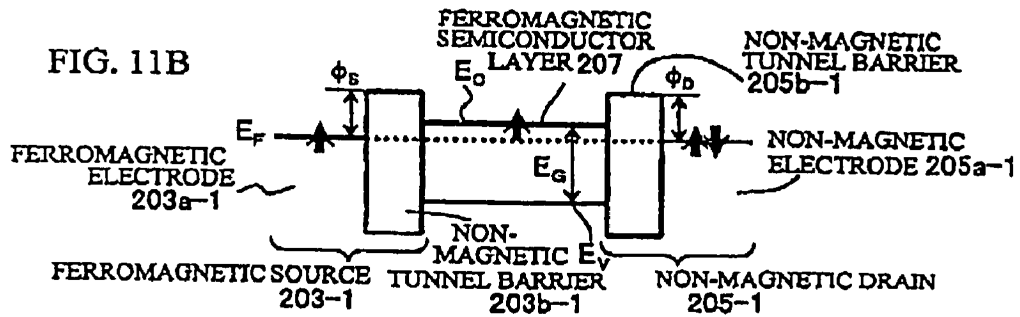

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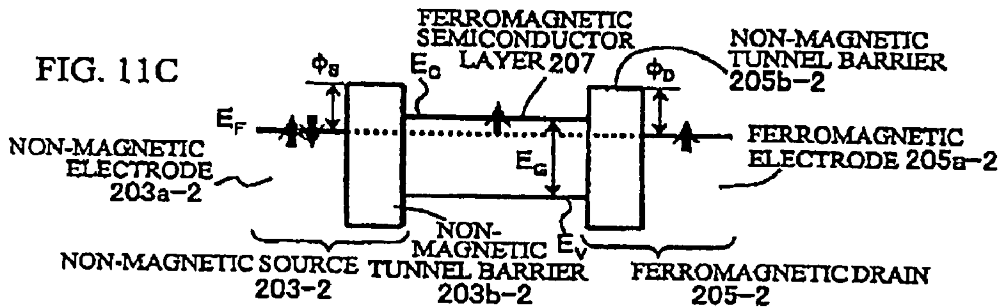


FIG. 11D

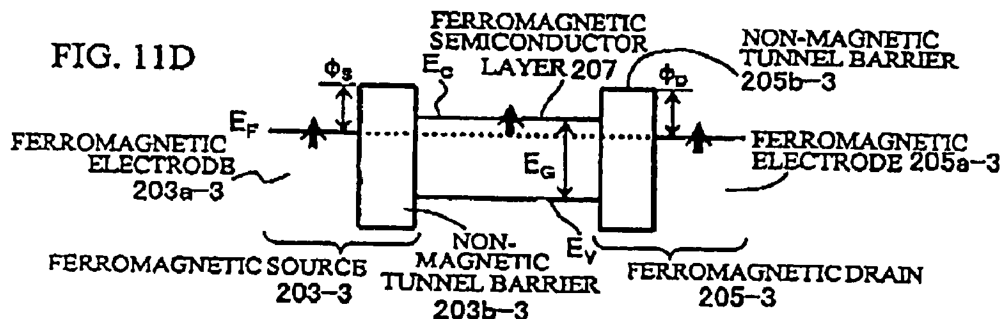
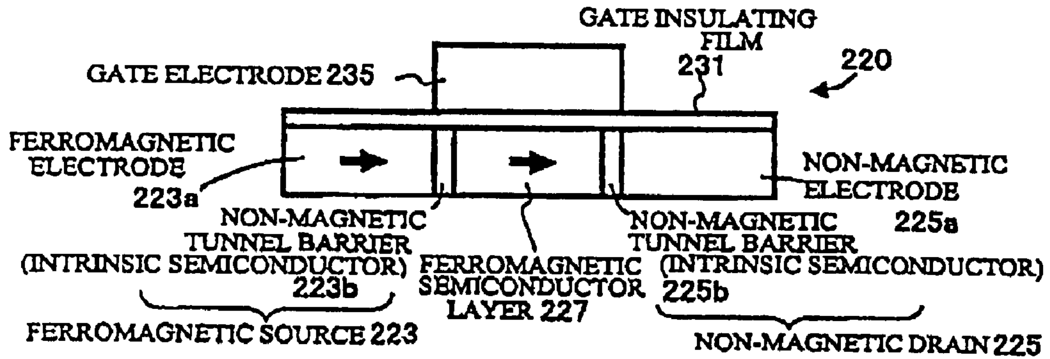


FIG. 12A



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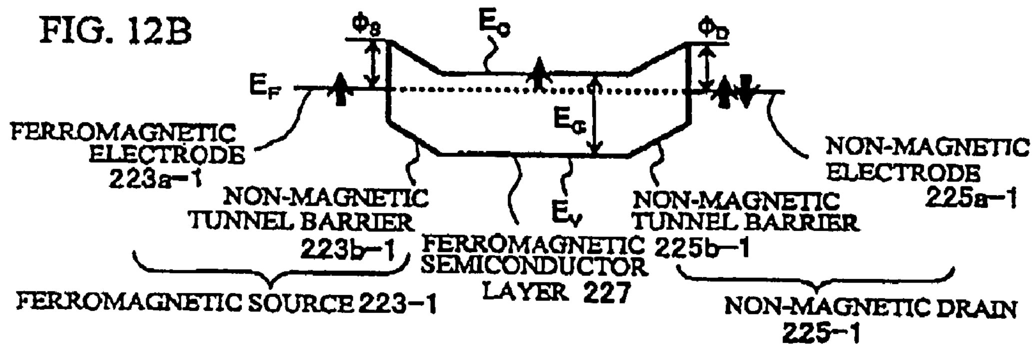

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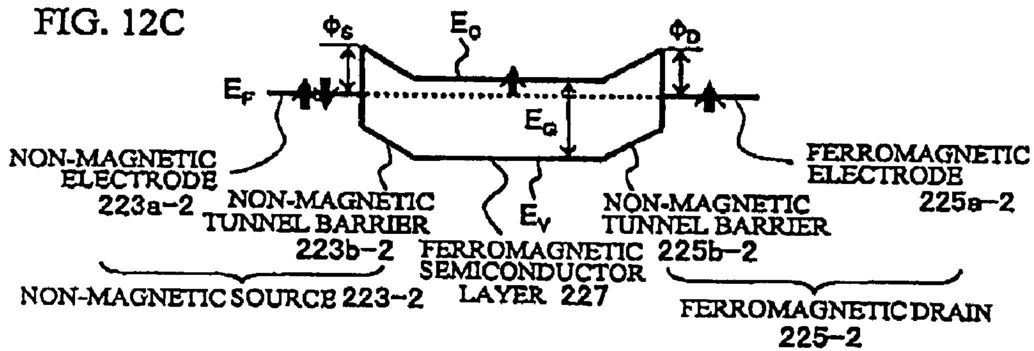

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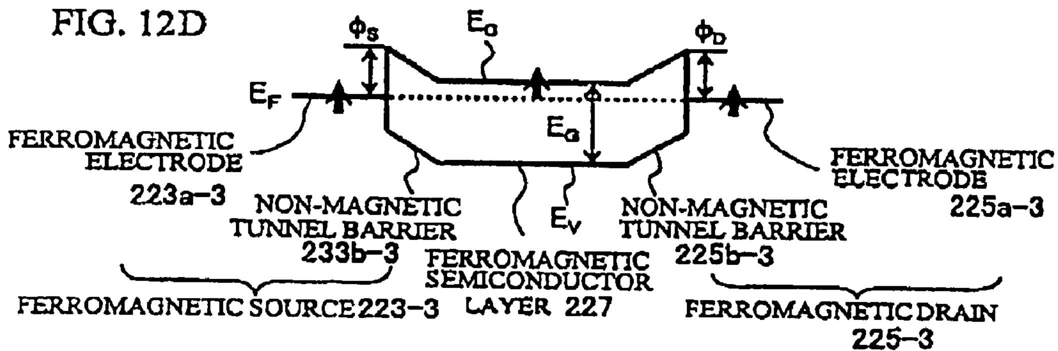

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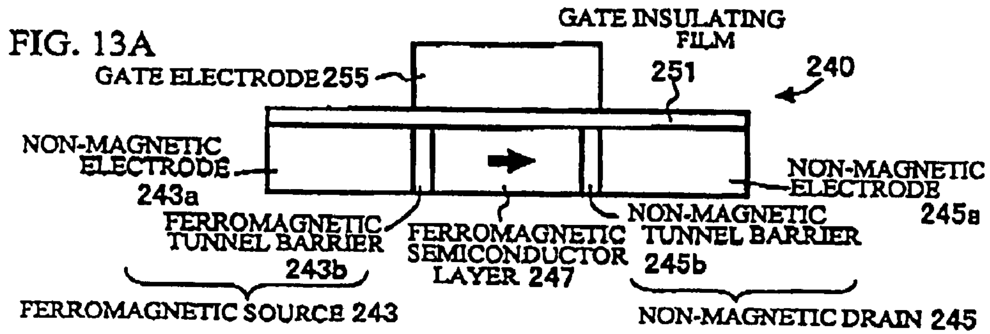

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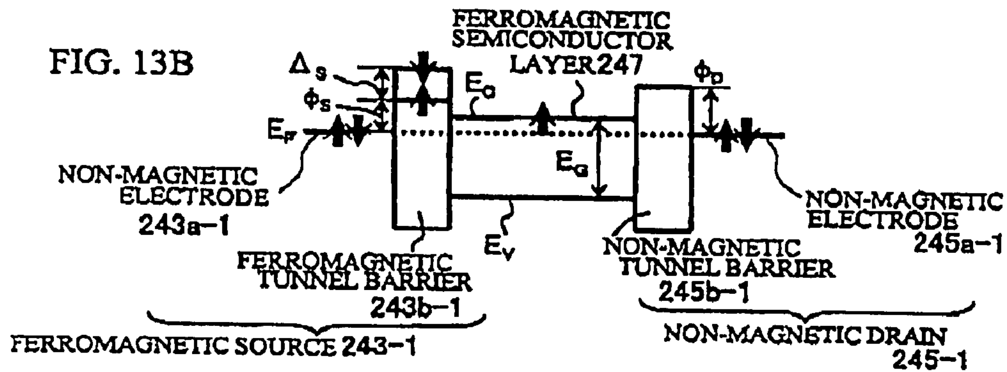

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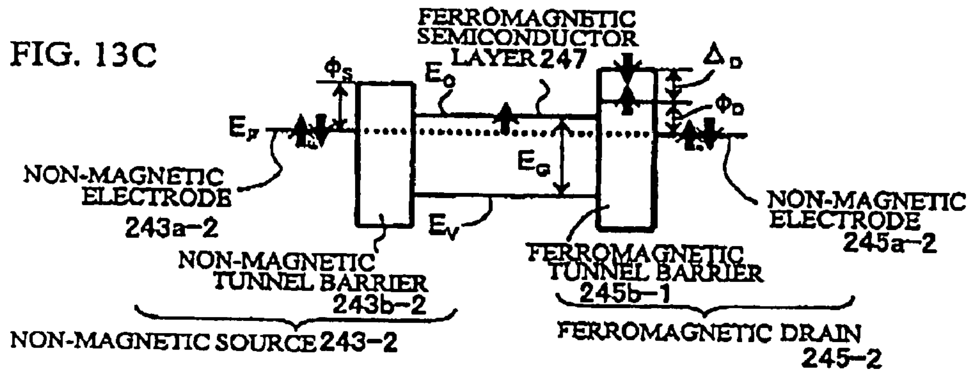
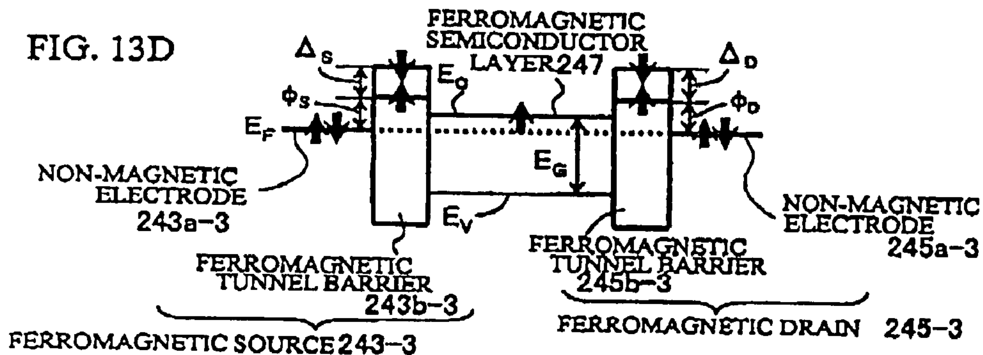


FIG. 13D



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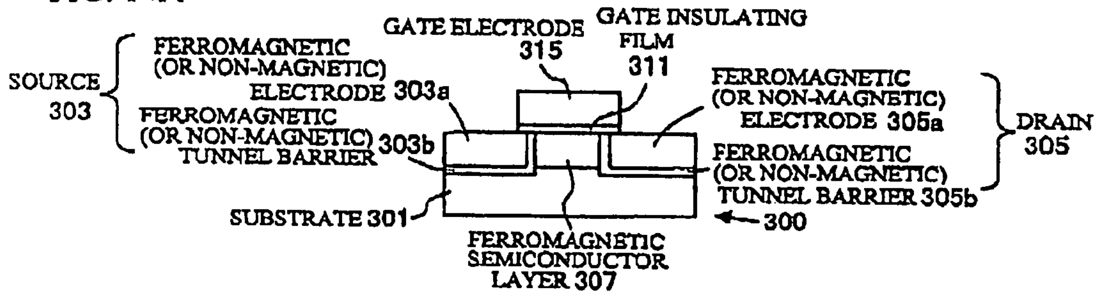
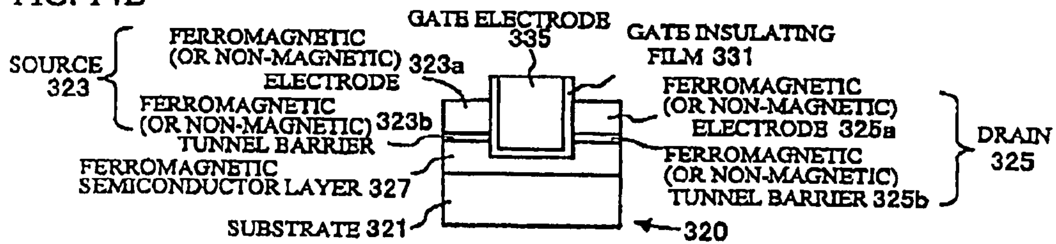


FIG. 14B



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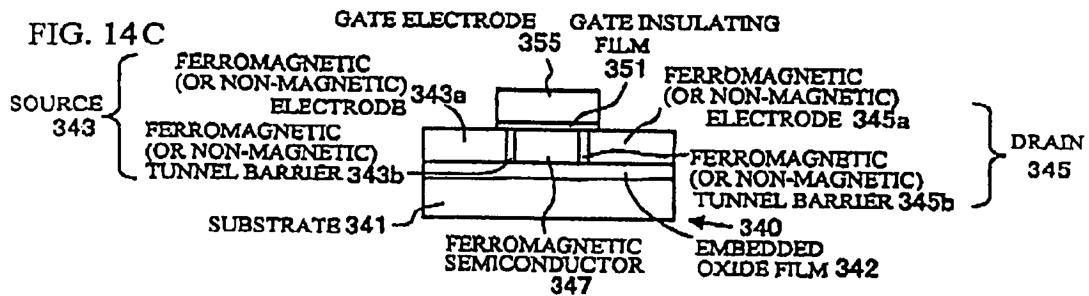


FIG. 14D

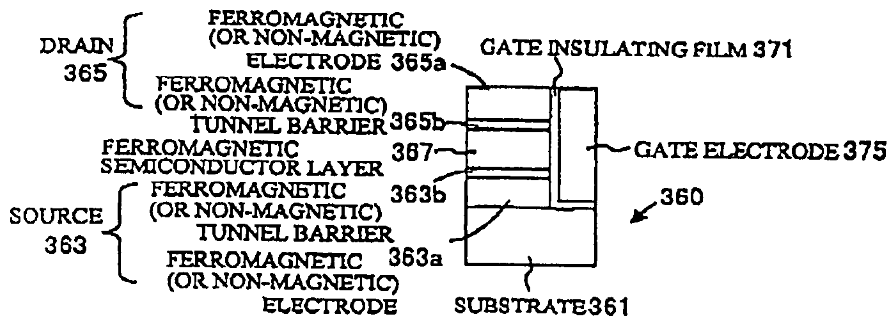


FIG. 15A

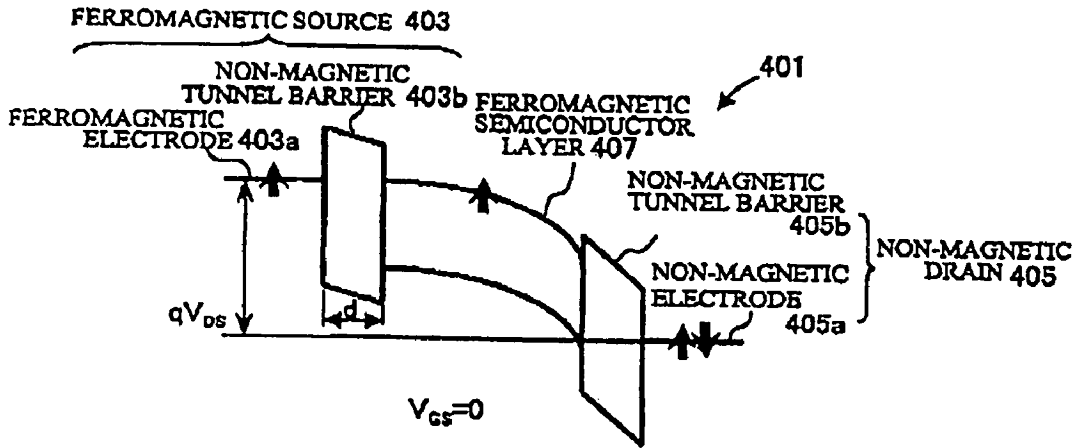


FIG. 15B

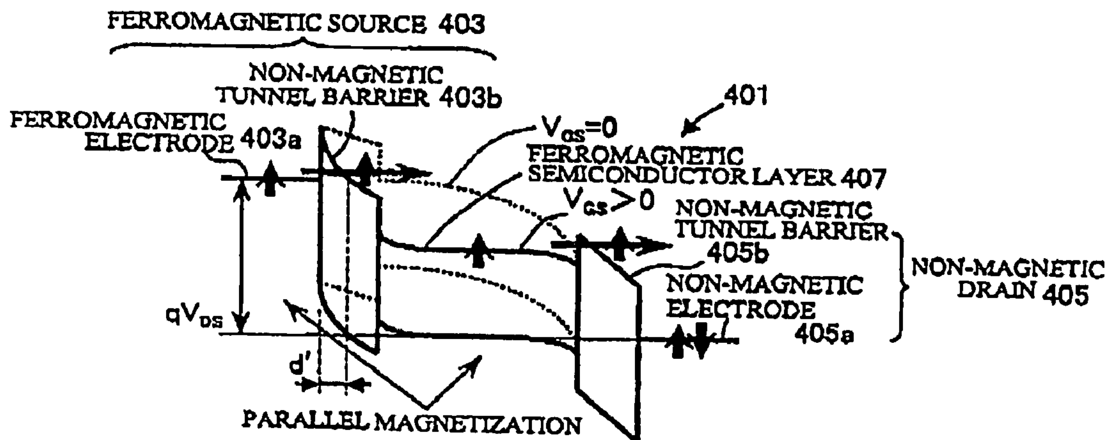


FIG. 15C

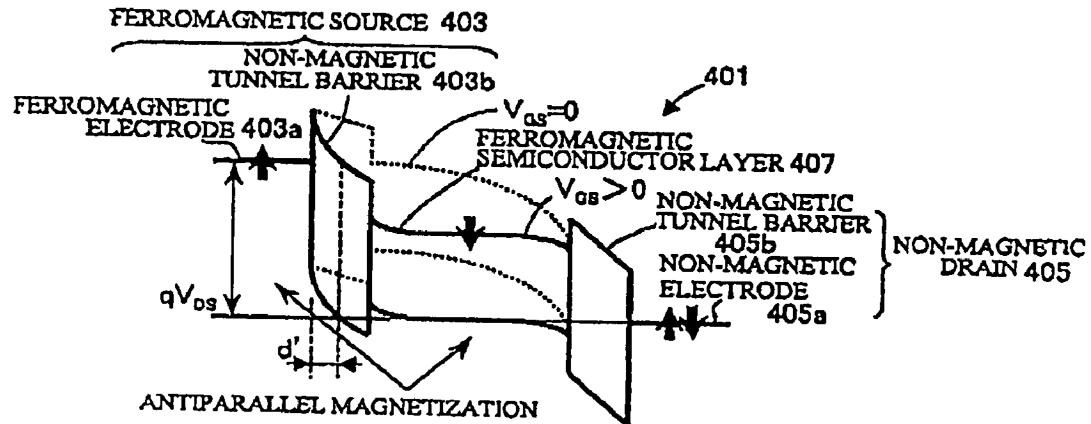
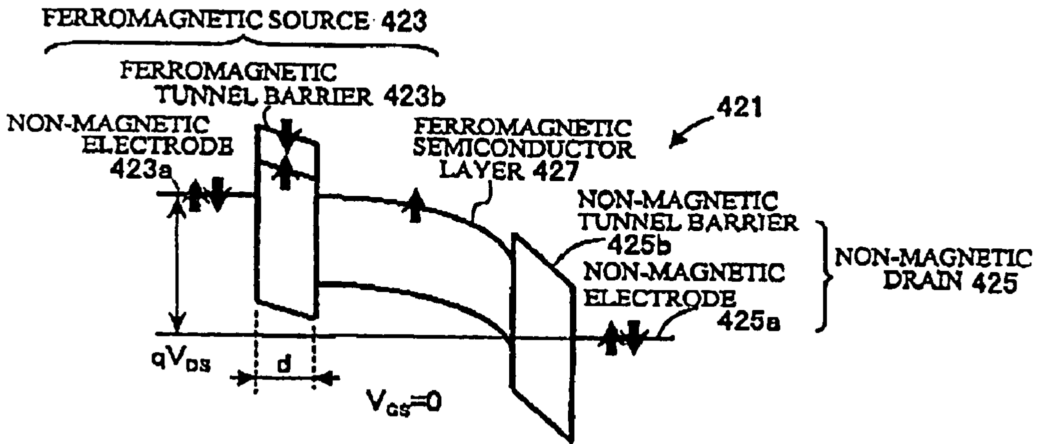


FIG. 16A



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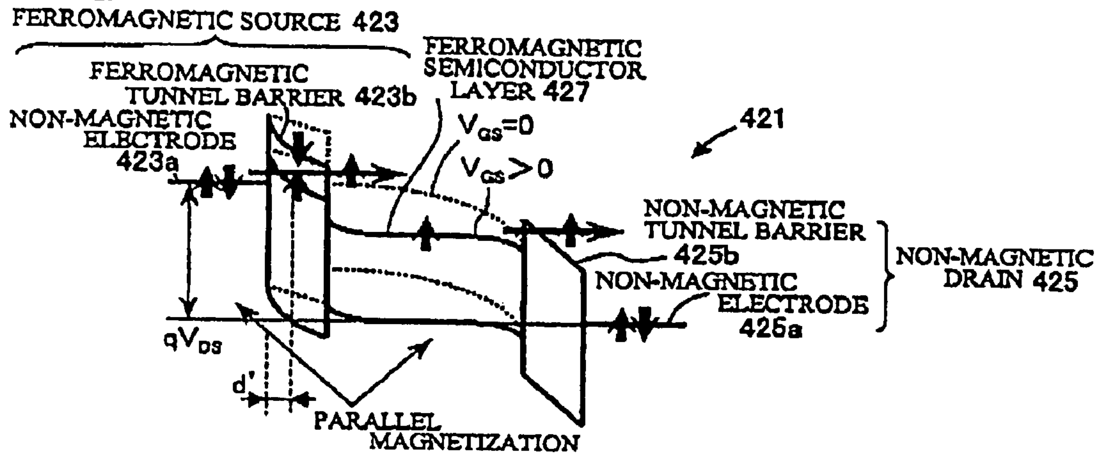


FIG. 16C

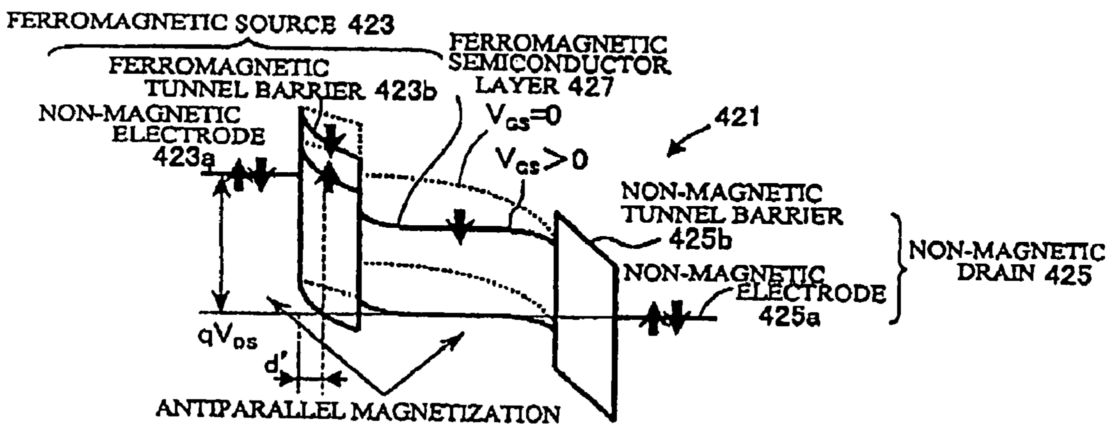


FIG. 17

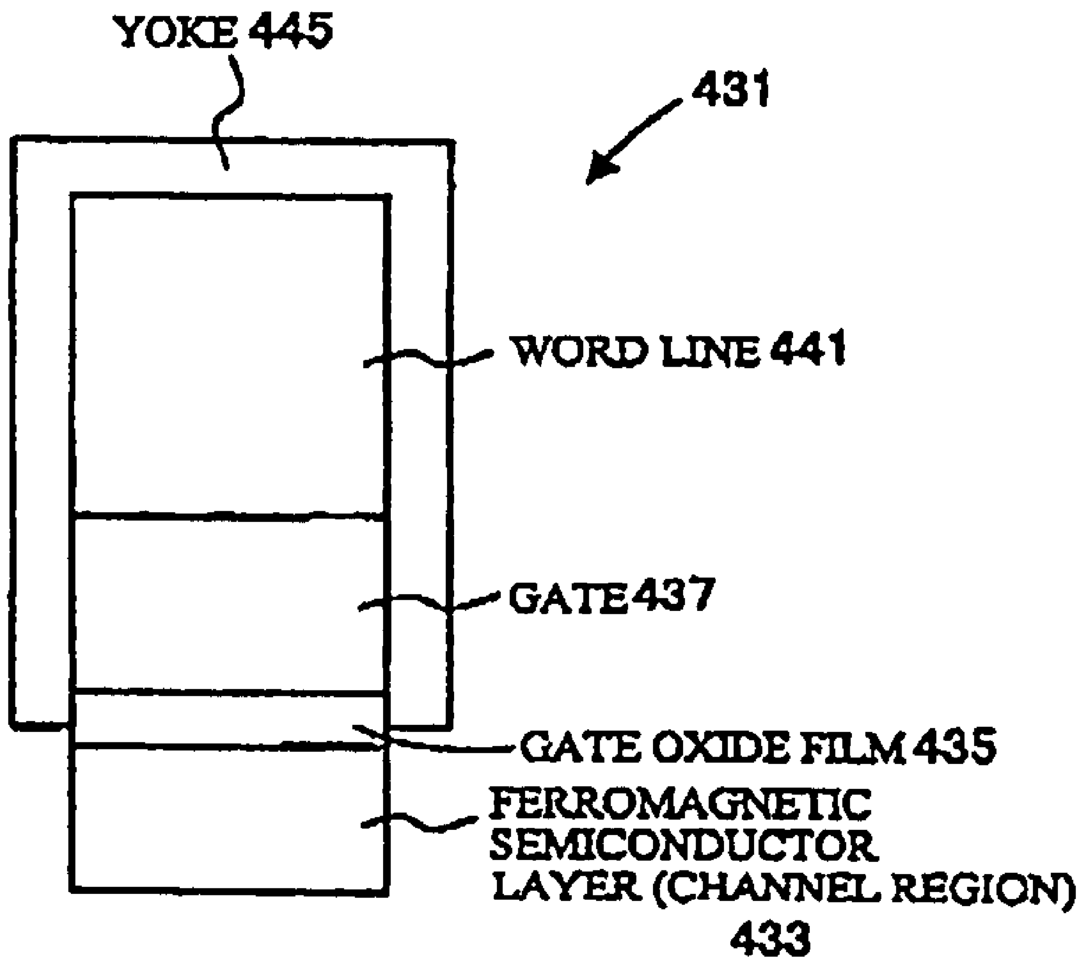


FIG. 18A

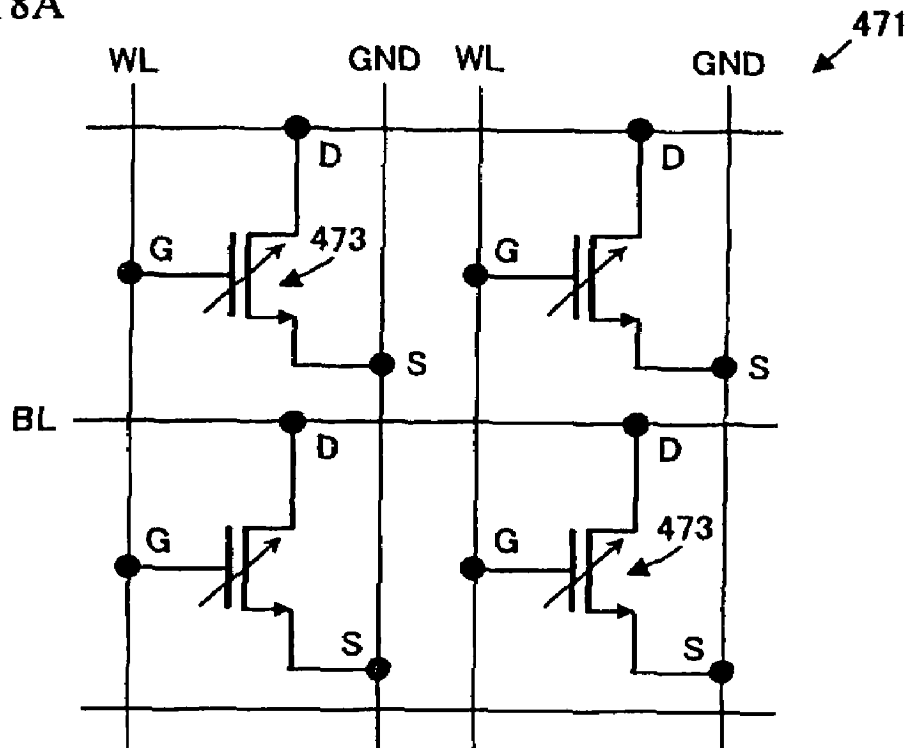


FIG. 18B

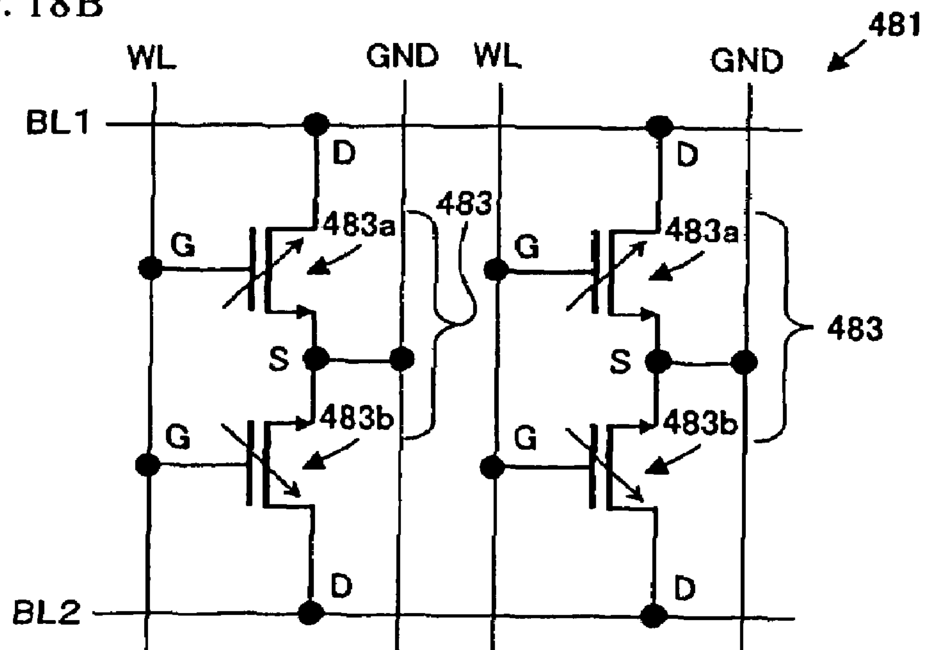


FIG. 19

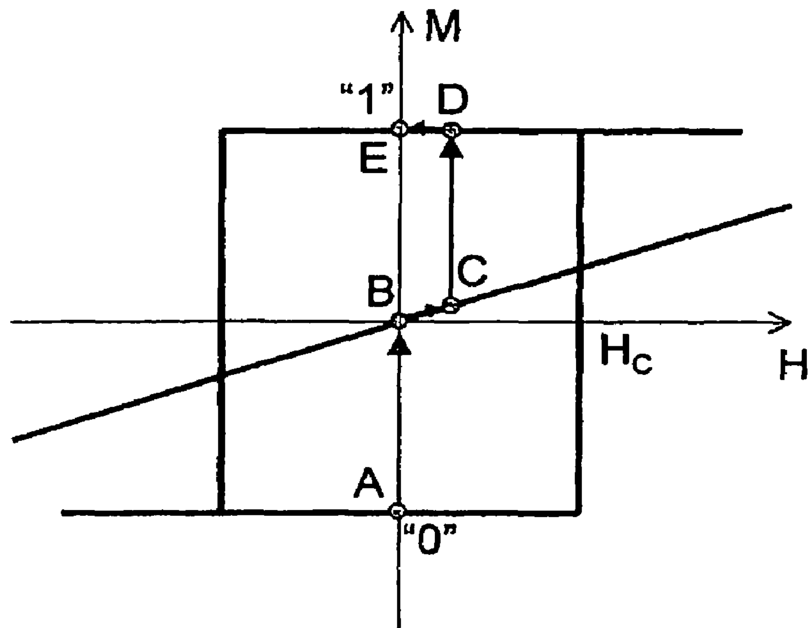


FIG. 20

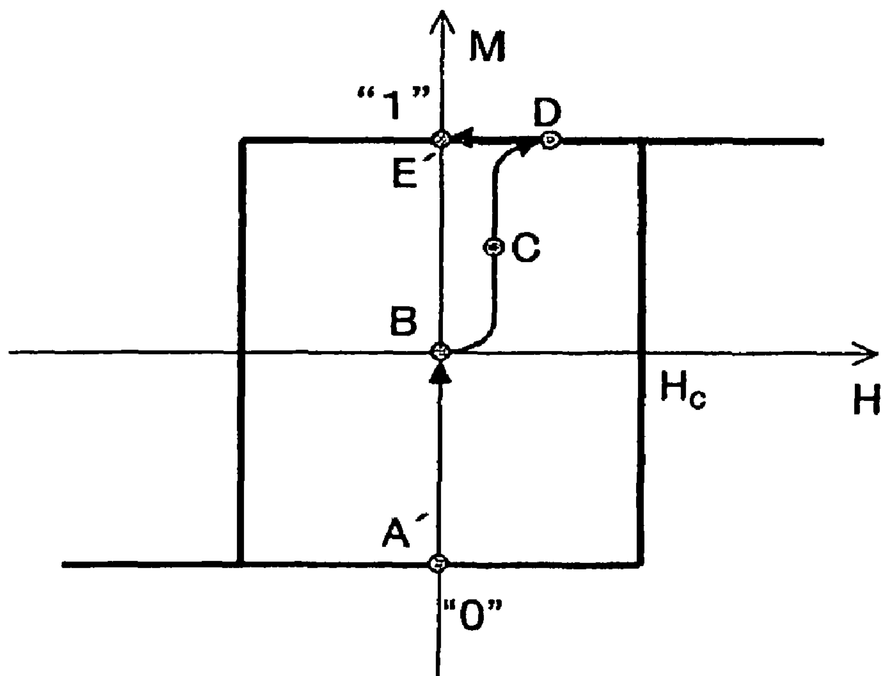
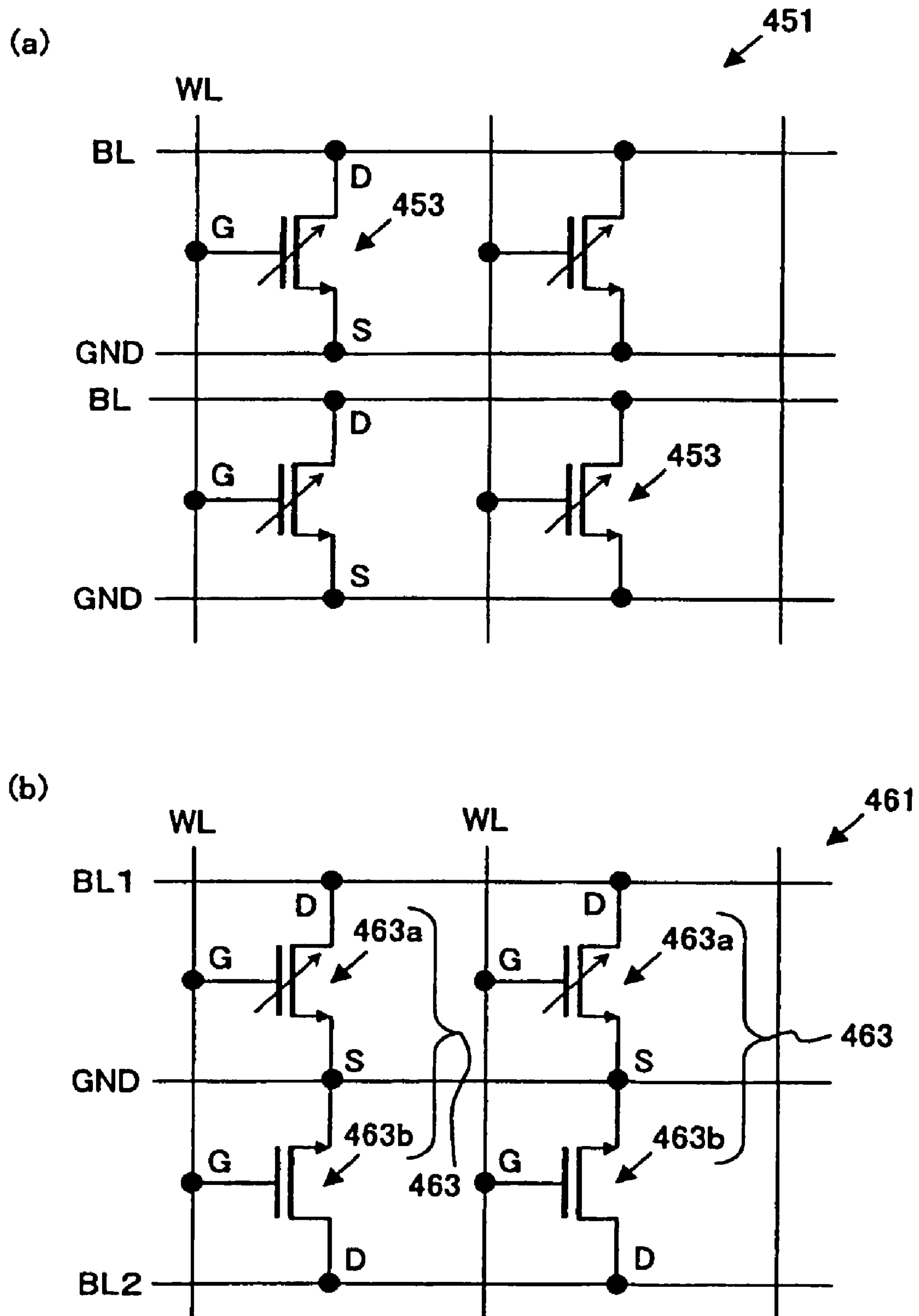


FIG. 21



TUNNEL TRANSISTOR HAVING SPIN-DEPENDENT TRANSFER CHARACTERISTICS AND NON-VOLATILE MEMORY USING THE SAME

This is a Division of application Ser. No. 10/551,802 filed Dec. 2, 2005 now U.S. Pat. No. 7,397,071. The disclosure of the prior application is hereby incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

The present invention relates to novel transistors, and more particularly, to a transistor with spin-dependent transfer characteristics and a non-volatile memory circuit (a non-volatile memory) using the transistor.

BACKGROUND OF THE INVENTION

Recent developments in the advanced information society are remarkable, and further rapid developments can be found in “mobile devices”. The great demand for the “mobile devices” is regarded as a possible main factor in future semiconductor industries. However, in addition to the existing demands for high-speed operations, low power consumption, and high capacities of semiconductor integrated circuits, there are new demands for non-volatility of information. In such a trend, attention has been drawn toward a novel memory device that has been developed by combining an excellent ferromagnetic storage technique and semiconductor integration electronics for non-volatile high-density recording (disclosed in Non-Patent Document 1, for example). This device is called a magneto-resistive random access memory (hereinafter referred to as “MRAM”), and a magnetic tunnel junction (hereinafter referred to as “MTJ”) having a thin insulating tunnel barrier interposed between ferromagnetic electrodes is used as a memory element.

A MTJ has a tunneling magneto-resistance (hereinafter referred to as “TMR”) effect with which the tunnel resistance varies with the relative magnetization direction between the ferromagnetic electrodes. Accordingly, using the MTR effect, the magnetization configuration of a ferromagnetic member can be electrically detected. With a MTJ, the non-volatile information using ferromagnetic members can be positively applied to the semiconductor integration electronics.

Referring now to FIG. **8**, an example of the prior art is described. As shown in FIG. **8**, an MRAM memory cell **100** has a 1-bit memory cell formed with a MTJ **101** and a MOS transistor **103**. The MTJ **101** is a tunnel junction that includes a first ferromagnetic electrode **105**, a second ferromagnetic electrode **107**, and a tunnel barrier **108** formed with an insulator interposed between the two electrodes.

The source (S) of the MOS transistor **103** is grounded (GND), and the drain (D) is connected to the ferromagnetic electrode **107** of the MTJ **101** with a plug PL. The ferromagnetic electrode **105** of the MTJ **101** is connected to a bit line BL. A rewrite word line **111** is disposed to cross the bit line at right angles, while being electrically insulated from the MTJ **101** and the other lines by an insulating film **115** immediately above or below the MTJ **101**. A read word line WL is connected to the gate electrode G of the MOS transistor **103**.

Since the magnetization directions can be maintained in a non-volatile manner in a ferromagnetic member, a MTJ can store binary information in a non-volatile manner by switching the relative magnetization configuration of the ferromagnetic electrodes to parallel magnetization or antiparallel magnetization. Also, in a MTJ, the tunnel resistance varies in accordance with the relative magnetization configuration between the two ferromagnetic electrodes due to the TMR effect. Accordingly, utilizing the tunnel resistance in accordance with the magnetization configuration that switches between parallel magnetization and antiparallel magnetization, the magnetization configuration of the MTJ can be electrically detected.

Information rewrite is performed by making the coercive forces of the two ferromagnetic electrodes **105** and **107** different from each other in the MTJ **101**, or inverting the magnetization of the ferromagnetic electrode with the smaller coercive force or with an unfixed magnetization direction while fixing the magnetization direction of the other ferromagnetic electrode. Hereinafter, a ferromagnetic member having a magnetization direction to be inverted will be referred to as a free layer, and a ferromagnetic member having a magnetization direction not to be inverted will be referred to as a pin layer. More specifically, currents are applied to the bit line BL and the rewrite word line **111** that cross each other on a selected memory cell. Using the synthetic magnetic field of the magnetic fields induced by the currents, only the magnetization configuration of the MTJ **101** in the selected memory cell **100** is switched to parallel magnetization or antiparallel magnetization. Here, the values of the currents to be applied to the lines are set so that the magnetization of the MTJ **101** of each unselected memory cell connected to the bit line BL and the rewrite word line **111** to which the selected memory cell is connected is not inverted only through one of the bit line BL and the rewrite word line **111**.

Information is read out by energizing the MOS transistor **103** through application of a voltage to the read word line WL connected to the selected cell, and then applying a read driving current to the MTJ **101** via the bit line BL. Since the tunnel resistance varies in accordance with the magnetization configuration that can be switched between parallel magnetization and antiparallel magnetization due to the TMR effect in the MTJ **101**, the magnetization configuration of the MTJ **101** can be determined by detecting a voltage decrease (hereinafter referred to as “output voltage”) due to the read driving current in the MTJ **101**. The following is the documents relating to the above described techniques.

1) K. Inomata, “Present and Future of Magnetic RAM Technology”, IEICE Trans. Electron., Vol. E84-C, 2001, pp. 740-746.

2) H. Ohno, D. Chiba, F. Matsukura, T. Omiya, E. Abe, T. Dietl, Y. Ohno, and K. Otani, “Electric-Field Control of Ferromagnetism”, Nature, Vol. 408, 2000, pp. 944-946. (also described later)

3) D. Chiba, M. Yamanouchi, F. Matsukura, and H. Ohno, “Electrical Manipulation of Magnetization Reversal in a Ferromagnetic Semiconductor”, Science, Vol. 301, 2003, pp. 943-945. (also described later)

DISCLOSURE OF THE INVENTION

(1) Information Reading

The problems with information (data) reading from a MRAM mainly derive from MTJs. A MTJ has a binary resistance value that depends on whether the relative magnetization configuration between the ferromagnetic electrodes interposing a tunnel barrier is parallel or antiparallel. So as to detect the binary data with a driving current with high sensitivity, it is necessary to optimize the output voltage by adjusting the impedance (the junction resistance) of the MTJ.

Furthermore, so as to read out the contents of stored information with high precision, it is necessary to set a high output signal ratio between the two magnetization configurations of

parallel magnetization and antiparallel magnetization. Therefore, the change rate in the TMR (also referred to as the TMR ratio) in each of the cases of parallel magnetization and antiparallel magnetization needs to be made higher in the MTJ. The TMR ratio depends on the spin polarization rate P of the ferromagnetic electrodes. So as to increase the TMR ratio, a ferromagnetic material with a large P value needs to be employed for the ferromagnetic electrodes.

The TMR ratio in a MTJ also depends on the voltage to be applied to the MTJ, and greatly decreases with a decrease of the voltage. When a high driving current is applied to a MTJ to read out information at a high speed, the voltage decrease becomes larger in the MTJ, and the TMR ratio drops. In other words, a high TMR ratio is traded for high-speed performance. Therefore, it is necessary to provide the TMR ratio with a bias resistance so as to prevent the TMR ratio from dropping with a large voltage decrease in the MTJ.

In view of the above facts, a memory element to be used for a MRAM preferably has an output that greatly depends whether the relative magnetization configuration is parallel magnetization or antiparallel magnetization. In the case of parallel magnetization or antiparallel magnetization configuration, the memory element preferably generates a sufficiently large output that does not depend on a bias to be applied to the device.

(2) Information Rewrite

In a MRAM, information is rewritten by changing the magnetization configuration of a MTJ through a magnetic field induced by the current flowing through the bit line and the word line. With MRAMs, high-density integration and high performance can be realized through miniaturization of devices as in a conventional semiconductor integrated memory. However, as MTJs are miniaturized, the demagnetizing field of each ferromagnetic electrode becomes larger, and the field intensity required for magnetization inversion becomes higher. Accordingly, the current required for rewrite becomes higher. The current increase is so large that the reliability of the lines cannot be maintained as the lines are miniaturized, even if an aspect ratio is increased as much as possible. The field intensity required for rewrite can be lowered by reducing the coercive force of the ferromagnetic members. However, fatal errors such as false write are caused in such a case.

Therefore, it is necessary to employ a method of rewriting magnetization information through a magnetic field generated by a low current value, without a decrease in the coercive force of each ferromagnetic body used in the memory element.

(3) High-Density Integration

A MRAM is suitable for high-density integration, because it has a simple structure and a MTJ can be reduced to a nano-scale size. So as to achieve high integration with several gigabits or greater, the channel length of each MOS transistor is expected to be 0.1 μm or shorter. However, when miniaturized MTJs in conformity with such miniaturized transistors are to be integrated, the contacts and the multilayer lines occupy the cell area, resulting in difficulty of integrating them with a high density.

Therefore, memory cells with simpler structures suitable for high-density integration are desired.

An object of the present invention is to provide a novel transistor that can control the output characteristics according to the magnetization configuration of a ferromagnetic member contained in the transistor. Another object of the present invention is to provide a large-capacity, high-performance non-volatile memory in which each 1-bit memory cell is formed only with the transistor.

The first aspect of the present invention provides a transistor that includes: a source (a ferromagnetic source) that is made of a ferromagnetic material and injects conduction carriers; a drain that receives the conduction carriers injected from the ferromagnetic source; a tunnel barrier (a ferromagnetic tunnel barrier) that is disposed between the ferromagnetic source and the drain, which is made of a ferromagnetic material; and a gate electrode that is formed in relation to the ferromagnetic tunnel barrier, and controls the carrier conduction from the ferromagnetic source to the drain by inducing an electric field in the ferromagnetic tunnel barrier. In this transistor, the energy band edge of the conduction band in the ferromagnetic tunnel barrier is spin-split in a case where the conduction carriers are electrons. In a case where the conduction carriers are holes, the energy band edge of the valence band in the ferromagnetic tunnel barrier is spin-split.

In a case where the magnetization direction of the ferromagnetic tunnel barrier is the same as the magnetization direction of the ferromagnetic source (parallel magnetization) or the direction of the major spin in the ferromagnetic source is parallel to the spin direction at the spin split, the tunneling probability of the major-spin electrons as the conduction carriers of the ferromagnetic source tunneling the ferromagnetic tunnel barrier is preferably controlled by the voltage (a gate voltage) to be applied to the gate electrode. For example, in the case where the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization, the gate voltage is applied to the ferromagnetic tunnel barrier so as to reduce the effective thickness of the tunnel barrier. By doing so, the ferromagnetic tunnel barrier has such a thickness as to generate a current that causes the major-spin electrons of the ferromagnetic source to tunnel the ferromagnetic tunnel barrier.

Meanwhile, in a case where the magnetization direction of the ferromagnetic tunnel barrier is opposite to the magnetization direction of the ferromagnetic source (antiparallel magnetization) or the direction of the major spin in the ferromagnetic source is antiparallel to the spin direction at the spin-split energy band edge of the ferromagnetic tunnel barrier, the barrier height of the ferromagnetic tunnel barrier in relation to the major spin in the ferromagnetic source is higher by the width of the spin split at the energy band edge. As a result, the tunnel current generated between the ferromagnetic source and the drain is smaller than the tunnel current generated in the case of parallel magnetization. Accordingly, even with the same biases being applied, the mutual (trans) conductance varies in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier.

The first aspect of the present invention also provides a memory circuit that includes: transistors that are arranged in a matrix fashion; first lines that ground the ferromagnetic sources; word lines that are collectively connected to the gate electrodes of the transistors aligned in the column direction; and bit lines that are collectively connected to the drains of the transistors aligned in the row direction.

The memory circuit may further include first extra lines and second extra lines that cross each other at right angles on the transistors, and are electrically insulated from each other. Also, the first extra lines and the second extra line may be replaced with the word lines and the bit lines. Alternatively, either the first extra lines or the second extra lines may be replaced with either the word lines or the bit lines.

In the above memory circuit, information stored in accordance with the magnetization direction can be rewritten by inverting the magnetization of the ferromagnetic source or the ferromagnetic tunnel barrier so as to change the relative mag-

netization configuration between the ferromagnetic source and the ferromagnetic tunnel barrier, using a magnetic field induced by applying current to the first extra line and the second extra line, or the word line and the bit line replacing the first extra line and the second extra line, or either the first extra line or the second extra line, or the word line or the bit line replacing either the first extra line or the second extra line and the first extra line or the second extra line, whichever is not replaced.

Information can be read out based on the output characteristics of the transistor in a case where a first bias is applied to the word line and a second bias is applied between the first line and the bit line.

The above memory circuit may further include: an output terminal formed at one end of each of the bit lines; and second lines that branch out from the bit lines and are connected to a power source via a load. In this case, information can be read out in accordance with an output voltage representing the voltage decrease in the load due to the current generated between the power source and the first line via the load and the transistor, with a first bias being applied to the word line.

Using the above circuit, a non-volatile memory circuit that is suitable for high-density integration and can have an output voltage that is formed with a power source and a load and varies in accordance with the magnetization configuration in the transistor can be provided.

Since the spin selecting rate in the ferromagnetic tunnel barrier in the transistor in accordance with the first aspect of the present invention, the change rate of current between parallel magnetization and antiparallel magnetization can be made higher. Furthermore, the single transistor serves as a non-volatile memory cell. Accordingly, a memory circuit using the above transistor can eliminate the above described problems in data reading and high-density integration.

The second aspect of the present invention provides a transistor that includes: a ferromagnetic semiconductor layer; a source that injects carriers into the ferromagnetic semiconductor layer; a drain that receives the carriers injected into the ferromagnetic semiconductor layer; and a gate electrode that applies a voltage for controlling the conduction of the carriers from the source to the drain. In this transistor, either one of the source and the drain is a ferromagnetic source or a ferromagnetic drain that includes a tunnel barrier (a "non-magnetic tunnel barrier") that is made of a non-magnetic material and is joined to the semiconductor layer, and an electrode (a "ferromagnetic electrode") that is made of a ferromagnetic material and is joined to the non-magnetic tunnel barrier. In the case where the source is the ferromagnetic source, the drain is a non-magnetic drain that includes a non-magnetic tunnel barrier joined to the semiconductor layer, and an electrode (a "non-magnetic electrode") that is made of a non-magnetic material and is joined to the non-magnetic tunnel barrier. In the case where the drain is the ferromagnetic drain, the source is a non-magnetic source that includes a non-magnetic tunnel barrier joined to the semiconductor layer, and a non-magnetic electrode joined to the non-magnetic tunnel barrier. Further, each of the source and the drain may include a non-magnetic tunnel barrier joined to the semiconductor layer, and a ferromagnetic electrode joined to the non-magnetic tunnel barrier. Each of the ferromagnetic source and the ferromagnetic drain may include a tunnel barrier (a "ferromagnetic tunnel barrier") that is made of a ferromagnetic material and is joined to the ferromagnetic semiconductor layer, and a non-magnetic electrode that is joined to the ferromagnetic tunnel barrier. In the case where the carriers are electrons, the energy barrier by the ferromagnetic tunnel barrier or the non-magnetic tunnel barrier is formed at least on the side of the conduction band. In the case where the carriers are holes, the energy barrier is formed at least on the side of the valence band.

The second aspect of the present invention also provides a memory circuit that includes: transistors that are arranged in a matrix fashion; ground lines that are collectively connected to the sources of the transistors aligned in the column direction; word lines that are collectively connected to the gate electrodes of the transistors aligned in the column direction; and bit lines that are collectively connected to the drains of the transistors aligned in the row direction.

The information stored in a transistor selected through the word line and the bit line can be rewritten by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a first state that is a paramagnetic state or a ferromagnetic state with sufficiently small coercive force, applying a current to the word line to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer in the first state, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state with large coercive force.

Information rewrite can also be performed by applying such a voltage to the bit line and the ground line that the ferromagnetic semiconductor layer is put into to a demagnetized state, applying a current to the word line to induce such a magnetic field as to magnetize the ferromagnetic semiconductor layer, and utilizing the initial magnetization characteristics after the application of the first voltage is cut off.

The information stored in a transistor selected through the word line and the bit line can be read out based on the intensity of a current flowing between the word line and the ground line, in a case where predetermined voltages are applied to the bit line and the word line, with the ground line being the reference.

The second aspect of the present invention also provides a memory circuit that includes: the transistors that are arranged in a matrix fashion; ground lines that are collectively connected to the sources of the transistors aligned in the row direction; word lines that are respectively connected to the gate electrodes of the transistors aligned in the column direction; and bit lines that are collectively connected to the drains of the transistors aligned in the row direction. In this circuit, the information stored in the transistors that are connected to the bit line and the ground line can be collectively rewritten by applying a first voltage to the bit line and the ground line so that the ferromagnetic semiconductor layer changes from a ferromagnetic state with large coercive force to a first state that is a paramagnetic state or a ferromagnetic state with sufficiently small coercive force, applying a current simultaneously to the word lines to induce such a magnetic field as to change the magnetization direction of the ferromagnetic semiconductor layer in the first state, and then cutting off the application of the first voltage or applying a second voltage so as to return the ferromagnetic semiconductor layer to the ferromagnetic state with the large coercive force.

The features of the memory circuit using the transistors in accordance with the second aspect of the present invention are as follows:

1) Information Write

A ferromagnetic semiconductor can be changed from a ferromagnetic state to a paramagnetic state by reducing the number of carriers in the ferromagnetic semiconductor layer through application of an electric field. This is called the field-effect magnetism control (see Non-Patent Documents 2

and 3). In a memory cell employing the transistor in accordance with the second aspect of the present invention, a voltage is applied to the source and the drain, so as to change the channel region from a ferromagnetic state to a paramagnetic state (or a state with sufficiently small coercive force). In this situation, magnetization inversion is performed. Accordingly, rewrite can be performed with a sufficiently small magnetic field by virtue of the coercive force in the ferromagnetic state. Also, the number of carriers in the ferromagnetic semiconductor is reduced by applying a bias to the source and the drain. By doing so, the ferromagnetic semiconductor can be demagnetized. After the application of a bias is cut off, a magnetic field is applied to the demagnetized ferromagnetic semiconductor, and the ferromagnetic semiconductor is magnetized in accordance with the initial magnetization. Thus, the magnetization information can be rewritten with a smaller magnetic field than the coercive force in the ferromagnetic state.

2) Information Reading

In the transistor in accordance with the second aspect of the present invention, the magnetization configuration is read out through a conduction phenomenon that is similar to the tunneling magneto-resistance (TMR) effect between the ferromagnetic semiconductor layer as the channel and the ferromagnetic source (or between the ferromagnetic semiconductor layer and the ferromagnetic drain). The bias applied between the source and the drain is divided at the source junction and the drain junction. Accordingly, in the device in accordance with the present invention, the output signal (the drain current) ratio between parallel magnetization and antiparallel magnetization exhibits lower bias dependence than the output signal ratio obtained with a conventional MTJ. In this device, a read bias higher than the bias in a MTJ can be applied. Particularly, in a case where the source is made of a ferromagnetic material, the bias dependence is remarkably lower.

3) High-Density Integration

In accordance with the second aspect of the present invention, a 1-bit memory cell is formed with the single transistor alone. Accordingly, a very simple structure can be formed with respect to the lines. Thus, a layout that is suitable for miniaturization can be easily formed.

A memory cell using the conventional MRAM has a 1-MTJ, 1-transistor, 4-line structure (see FIG. **8**). Therefore, it is difficult to reduce the cell area by sharing a source between two adjacent cells, due to the existence of the MTJ and the write word line. With the memory cells in accordance with the present invention, on the other hand, a cell structure in which a source can be shared by two adjacent cells can be formed.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic cross-sectional view of a transistor in accordance with a first embodiment of the present invention;

FIG. **2**A shows the energy band structure in a case where the ferromagnetic source of the transistor of FIG. **1** is made of a ferromagnetic metal;

FIG. **2**B shows the energy band structure in a case where the ferromagnetic source is an n-type ferromagnetic semiconductor;

FIG. **2**C shows the energy band structure in a case where the ferromagnetic source is a p-type ferromagnetic semiconductor;

FIG. **3**A illustrates the operation principle of the transistor of this embodiment, showing the energy band structure in a case where a gate voltage is not applied;

FIG. **3**B shows the energy band structure in a case where a gate voltage is applied and the ferromagnetic source and the ferromagnetic tunnel barrier exhibit parallel magnetization;

FIG. **3**C shows the energy band structure in a case where a gate voltage is applied and the ferromagnetic source and the ferromagnetic tunnel barrier exhibit antiparallel magnetization;

FIG. **4** shows the output characteristics of the transistor shown in FIG. **1** and FIGS. **2**A through **2**C;

FIG. **5** is a cross-sectional view illustrating an example structure of a transistor in accordance with a second embodiment of the present invention;

FIG. **6** is a cross-sectional view of an example structure of a transistor in accordance with a fourth embodiment of the present invention;

FIGS. **7**A and **7**B illustrates memory circuits in accordance with a fifth embodiment and a sixth embodiment of the present invention, with one of the transistors in accordance with the first through fourth embodiments of the present invention being employed in each of the memory circuits;

FIG. **7**C shows the output characteristics of the memory circuit shown in FIG. **7**B;

FIG. **8** is a cross-sectional view of a memory cell of a conventional MRAM using MTJ;

FIG. **9** is a cross-sectional view of an example structure of a memory cell having a shared ferromagnetic source;

FIG. **10** is a cross-sectional view of an example structure of a memory cell using the transistor in accordance with the fourth embodiment of the present invention;

FIG. **11**A illustrates the structure of a MISFET having a ferromagnetic semiconductor layer as a channel region in accordance with a seventh embodiment of the present invention;

FIGS. **11**B through **11**D show band structures in the vicinity of the channel region of the MISFET of the seventh embodiment at the time of thermal equilibrium;

FIGS. **12**A through **12**D illustrate example device structures of MISFETs each having a ferromagnetic semiconductor layer as a channel region in accordance with an eighth embodiment of the present invention;

FIGS. **13**A through **13**D illustrate the structures of MISFETs each having a ferromagnetic semiconductor layer as a channel region in accordance with a ninth embodiment of the present invention;

FIGS. **14**A through **14**D illustrate the device structures of MISFETs in accordance with tenth through thirteenth embodiments of the present invention;

FIG. **15**A illustrates the operation principles of the transistor of the seventh embodiment, showing the energy band structure in a case where a gate voltage is not applied;

FIG. **15**B illustrates the operation principles of the transistor of the seventh embodiment, showing the energy band structure in a case where a gate voltage is applied and the ferromagnetic source and the ferromagnetic semiconductor layer exhibit parallel magnetization;

FIG. **15**C illustrates the operation principles of the transistor of the seventh embodiment, showing the energy band structure in a case where a gate voltage is applied and the ferromagnetic source and the ferromagnetic semiconductor layer exhibit antiparallel magnetization;

FIG. **16**A illustrates the operation principles of the transistor of the ninth embodiment, showing the energy band structure in a case where a gate voltage is not applied;

FIG. **16**B illustrates the operation principles of the transistor of the ninth embodiment, showing the energy band structure in a case where a gate voltage is applied and the ferro-

magnetic source and the ferromagnetic semiconductor layer exhibit parallel magnetization;

FIG. **16**C illustrates the operation principles of the transistor of the ninth embodiment, showing the energy band structure in a case where a gate voltage is applied and the ferromagnetic source and the ferromagnetic semiconductor layer exhibit antiparallel magnetization;

FIG. **17** illustrates a MISFET in accordance with a fourteenth embodiment of the present invention, showing a compound structure of a gate electrode and a word line utilizing a yoke;

FIG. **18**A illustrates an example memory cell structure of a non-volatile memory in accordance with a fifteenth embodiment of the present invention, using MISFETs of one of the seventh through fourteenth embodiments;

FIG. **18**B illustrates an example memory cell structure of a non-volatile memory in accordance with a sixteenth embodiment of the present invention, using MISFETs of one of the seventh through fourteenth embodiments;

FIG. **19** shows a magnetization curve representing the principles of memory cell rewrite operation utilizing the field-effect magnetization control of the ferromagnetic semiconductor layer;

FIG. **20** shows a magnetization curve representing the principles of memory cell rewrite operation utilizing the initial magnetization characteristics of the ferromagnetic semiconductor layer;

FIG. **21**A illustrates a memory cell structure in accordance with a seventeenth embodiment of the present invention; and

FIG. **21**B illustrates a memory cell structure in accordance with an eighteenth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A transistor in accordance with a first aspect of the present invention is a novel transistor that utilizes the spin-dependent tunnel effect caused by the junction between a ferromagnetic source and a ferromagnetic tunnel barrier. More specifically, the transistor is formed with a tunnel junction structure having an insulating ferromagnetic tunnel barrier interposed between a ferromagnetic source and a drain, and a gate electrode that is formed in relation to the ferromagnetic tunnel barrier and can induce an electric field in the ferromagnetic tunnel barrier.

Although the term "spin" is generally used for spin angular momentum, it will also refer to carriers with predetermined spin directions in the following description. The magnetization direction of each ferromagnetic tunnel barrier is determined by the spin direction of the spin band at the energy band edge (for example, if the band edge of a conduction band is spin-split, the magnetization direction is opposite to the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier).

Since the up-spin band and the down-spin band are spin-split at the band edge of the ferromagnetic tunnel barrier, the barrier height of the tunnel barrier seen from the ferromagnetic source varies between the up spin and the down spin. Accordingly, the tunneling probability of the ferromagnetic tunnel barrier depends on the spin direction of the carriers in the ferromagnetic source. A gate voltage is applied to the ferromagnetic tunnel barrier to change the potential shape of the ferromagnetic tunnel barrier. By doing so, the tunneling probability is changed, and the tunnel current generated between the ferromagnetic source and the drain is controlled. Accordingly, the size of the tunnel current depends on the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier in relation to the spin direction of the major-spin electrons in the ferromagnetic source. In other words, the size of the tunnel current depends on the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier.

The magnetization in a case where the spin direction of the major-spin electrons in the ferromagnetic source is the same as the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier is referred to as "parallel magnetization", while the magnetization in a case where those spin directions are opposite to each other is referred to as "antiparallel magnetization". In the case of parallel magnetization, the barrier height of the ferromagnetic tunnel barrier seen from the major-spin electrons of the ferromagnetic source is low, and a drain current can be easily generated by a gate voltage. In the case of antiparallel magnetization, on the other hand, the barrier height of the ferromagnetic tunnel barrier seen from the major-spin electrons of the ferromagnetic source is high, and the drain current is lower than the drain current in the case of parallel magnetization, even if the same bias as the bias applied in the case of parallel magnetization is applied. Accordingly, the above transistor has mutual (trans) conductance that varies in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier.

The above transistor stores information by changing the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier with a magnetic field or the like, and is capable of electrically reading out the stored information by virtue of the transfer characteristics of the transistor. Thus, a 1-bit non-volatile memory cell can be formed with the above transistor alone.

Based on the above discussion, embodiments of the present invention will be described below in conjunction with the accompanying drawings. First, a transistor in accordance with a first embodiment of the present invention is described.

FIG. **1** is a cross-sectional view of an example structure of the transistor in accordance with the first embodiment of the present invention. As shown in FIG. **1**, the transistor **1** in accordance with this embodiment includes a tunnel function structure and a control electrode structure. The tunnel junction structure includes the functions among a ferromagnetic source **3**, a ferromagnetic tunnel barrier **7**, and a drain **5**. The control electrode structure includes a gate insulating film **11** and a gate electrode **15** formed in relation with the ferromagnetic tunnel barrier **7**, and can apply an electric field to the ferromagnetic tunnel barrier **7**. The tunnel junction structure and the control electrode structure constitute the transistor **1**.

The ferromagnetic source is made of a ferromagnetic metal such as Ni, Co, Fe, and permalloy, or an electrically conductive ferromagnetic semiconductor such as a semiconductor containing GaMnAs, magnetic elements, or the likes. The ferromagnetic tunnel barrier is made of an insulating ferromagnetic semiconductor such as EuS, or a ferromagnetic insulator such as garnet. Alternatively, a ferromagnetic semiconductor that contains magnetic elements and exhibits insulation may be used for the ferromagnetic tunnel barrier. The drain may be made of a non-magnetic metal such as Al, Au, and non-magnetic silicide, or an electrically conductive non-magnetic semiconductor such as doped Si and GaAs. However, in a case where a ferromagnetic semiconductor and a non-magnetic semiconductor are used for the ferromagnetic source and the drain, respectively, the ferromagnetic semiconductor and the non-magnetic semiconductor need to have the same conductivity type.

If a ferromagnetic metal or an n-type ferromagnetic semiconductor is used for the ferromagnetic source, the conduc-

tion carriers serve as electrons, and the ferromagnetic tunnel barrier needs to have a spin-split bottom as the bottom of the conduction band. If a p-type ferromagnetic semiconductor is used for the ferromagnetic source, the conduction carriers serve as holes, and the top of the valence band in the ferromagnetic tunnel barrier needs to be spin-split.

FIG. **2**A illustrates an example of the energy band structure that is observed in a case where the ferromagnetic source and the drain of the transistor shown in FIG. **1** are formed with a ferromagnetic metal and a non-magnetic metal, respectively. The solid lines on the ferromagnetic source **3** and the drain **5**, and the broken line on the ferromagnetic tunnel barrier **7** indicate Fermi energy E_f. The two adjacent solid lines **21** and **25** at the bottom of the conduction band of the ferromagnetic tunnel barrier **7** indicate the band edges of the up-spin band and the down-spin band, respectively.

The upward-pointing arrows and the downward pointing arrow in the drawing indicate the up spin and the down spin. The arrow shown over the Fermi energy E_f of the ferromagnetic source indicates the orientation of the major-spin electrons, and the orientation of the minor-spin electrons is not shown. Likewise, an upward-pointing arrow and a downward-pointing arrow indicate the up-spin band edge **21** and the down-spin band edge **25** in the ferromagnetic tunnel barrier **7**. In the drain **5**, the two aligning upward-pointing and downward-pointing arrows shown on the Fermi energy E_f indicate that the drain **5** is a non-magnetic body. (In the other drawings, the upward-pointing and downward-pointing arrows in each region will imply the same as the above.)

In the drawing, Δ indicates the spin-split width between the up-spin band edge **21** and the down-spin band edge **25**. The barrier height of the ferromagnetic tunnel barrier **7** in relation to the ferromagnetic source **3** differs between the up spin and the down spin, and the greater height is denoted by ϕ. More specifically, the difference between the Fermi energy E_f of the ferromagnetic source **3** and the energy at the bottom of the spin band with the lowest energy in the conduction band in the ferromagnetic tunnel barrier **7** is denoted by ϕ.

FIG. **2**B illustrates an energy band structure that is observed in a case where the ferromagnetic source **3** and the drain **5** of the transistor **1** shown in FIG. **1** are formed with an n-type ferromagnetic semiconductor and an n-type non-magnetic semiconductor, respectively. The solid lines E_c on the ferromagnetic source **3***a* and the drain **5***a* indicate the energy at the bottom of the conduction band. The broken line shown across the ferromagnetic source **3***a*, the drain **5***a*, and the ferromagnetic tunnel barrier **7***a* indicates Fermi energy E_f.

As in the example shown in FIG. **2**A, Δ indicates the spin-split width between the up-spin band edge **21***a* and the down-spin band edge **25***a* in the ferromagnetic tunnel barrier, and the difference between the energy at the bottom of the conduction band of the ferromagnetic source **3***a* and the energy at the bottom of the spin band with the lowest energy in the conduction band in the ferromagnetic tunnel barrier **7***a* is denoted by ϕ. In FIG. **2**B, a non-degenerate ferromagnetic semiconductor and a non-magnetic semiconductor are employed. However, it is also possible to employ a degenerate ferromagnetic semiconductor and a non-magnetic semiconductor for the ferromagnetic source **3***a* and the drain **5***a*, respectively.

FIG. **2**C illustrates an energy band structure that is observed in a case where the ferromagnetic source **3** and the drain **5** of the transistor shown in FIG. **1** are formed with a p-type ferromagnetic semiconductor and a p-type non-magnetic semiconductor, respectively. The solid line E_v on the ferromagnetic source **3***b* and the drain **5***b* indicates the energy at the top of the valence band. The broken line shown across the ferromagnetic source **3***b*, the drain **5***b*, and the ferromagnetic tunnel barrier **7***b* indicates Fermi energy. The two adjacent solid lines existing at the top of the valence band of the ferromagnetic tunnel barrier **7***b* indicate the band edges of the up-spin band **21***b* and the down-spin band **25***b*, respectively. In FIG. **2**C, Δ indicates the spin-split width between the up-spin band **21***b* and the down-spin band **25***b*. The difference between the energy at the top of the valence band of the ferromagnetic source **3***b* the energy at the top of the spin band with the highest energy in the valence band in the ferromagnetic tunnel barrier **7***b* is denoted by ϕ. In the example shown in FIG. **2**C, a non-degenerate ferromagnetic semiconductor and a non-magnetic semiconductor are employed. However, it is also possible to employ a degenerate ferromagnetic semiconductor and a non-magnetic semiconductor for the ferromagnetic source **3***b* and the drain **5***b*, respectively.

The magnetization in the case where the direction of the major spin in the ferromagnetic source **3** is the same as the spin direction of the spin band that is the band edge of the ferromagnetic tunnel barrier **7** in FIG. **1** is "parallel magnetization". The magnetization in the case where those spin directions are opposite to each other is "antiparallel magnetization". The barrier thickness of the ferromagnetic tunnel barrier in relation to the major spin in the ferromagnetic source is ϕ in the case of parallel magnetization, but is ϕ+Δ in the case of antiparallel magnetization. Accordingly, the magnetization direction of the tunnel barrier **7** in relation to the ferromagnetic source **3** is changed from parallel magnetization to antiparallel magnetization by applying a magnetic field, for example. By doing so, the barrier height with respect to the major spin in the ferromagnetic source can be increased from ϕ to ϕ+Δ.

The thickness of the gate insulating film **11** should preferably be so thin as to change the potential of the ferromagnetic tunnel barrier with a voltage applied to the gate electrode, and should also preferably be so thick as not to cause leakage current (such as tunnel current) between the gate electrode **15** and the ferromagnetic source **3** or the drain **5** at the time of gate voltage application.

In the case where the ferromagnetic source and the ferromagnetic tunnel barrier exhibit parallel magnetization, the thickness of the ferromagnetic tunnel barrier is designed to be so thick as to cause almost no current due to a tunneling effect such as direct tunneling from the source to the drain or Fowler-Nordheim tunneling (hereinafter referred to as the "FN tunneling") when only a bias V_{DS} is applied between the ferromagnetic source **3** and the drain **5**. With this structure, when a bias V_{GS} is applied between the gate electrode **15** and the ferromagnetic source **3**, the potential shape caused by the application of V_{DS} at the band edge of the ferromagnetic tunnel barrier **7** is changed to cause a tunnel current.

In the following, the operation of the transistor in accordance with this embodiment is described in detail, with reference to FIGS. **3**A through **3**C. In the example case described below, a ferromagnetic metal is used for the ferromagnetic source and the conduction carriers are electrons, as shown in FIG. **2**A. If the ferromagnetic source **3** and the ferromagnetic tunnel barrier **7** exhibit parallel magnetization, the spin band of the spins parallel to the major spin in the ferromagnetic source **3** is the band edge of the ferromagnetic tunnel barrier **7**. Therefore, the barrier height seen from the major-spin electrons in the ferromagnetic source **3** is ϕ. When the bias V_{DS} is applied only between the source **3** and the drain **5**, the potential of the ferromagnetic tunnel barrier **7** changes from the rectangular form shown in FIG. **2**A to the shape shown in FIG. **3**A or a similar form to that. Here, the bias V_{DS} is of such a size that a current caused by the FN tunneling

hardly flows. More specifically, even if the Fermi energy of the ferromagnetic source **3** crosses the band edge of the ferromagnetic tunnel barrier **7** due to the application of V_{DS}, the distance d from the interface between the ferromagnetic source and the ferromagnetic tunnel barrier to the crossing point between the Fermi energy of the ferromagnetic source and the band edge of the ferromagnetic tunnel barrier is as long as not to cause FN tunneling.

When the bias V_{GS} (>0) is applied to the gate electrode, the electric field in the vicinity of the interface between the ferromagnetic source and the ferromagnetic tunnel barrier is intensified by the electric flux line from the gate electrode to the ferromagnetic source. The potential shape shown in FIG. **3**B is then formed. If the width of the potential barrier is reduced from the distance d, with which tunneling is hardly caused, to a distance d' with which tunneling can be caused, the ferromagnetic tunnel barrier **7** can transmit the major-spin electrons of the ferromagnetic source **3**. Thus, a drain current is generated between the ferromagnetic source **3** and the drain **5**. Meanwhile, the barrier height in relation to the minor-spin electrons of the ferromagnetic source **3** is greater than ϕ by Δ, and the carrier density of the minor-spin electrons is low. Therefore, the drain current generated by the minor-spin electrons is low. Accordingly, the drain current is equal to the sum of the tunnel current generated by the major-spin electrons and the tunnel current generated by the minor-spin electrons of the ferromagnetic source **3**. However, if the size of Δ is sufficiently large, the tunnel current generated by the major-spin electrons becomes dominant.

Since the tunneling probability dramatically increases with a decrease of the width of the tunnel barrier due to the bias V_{GS}, the drain current I_D greatly varies even with a minute change in the bias V_{GS}. Accordingly, high mutual (trans) conductance can be achieved.

In the case where the ferromagnetic source and the ferromagnetic tunnel barrier exhibit antiparallel magnetization as shown in FIG. **3**C, the barrier height in relation to the major spin in the ferromagnetic source is $\phi+\Delta$, and the barrier height in relation to the minor-spin electrons of the ferromagnetic source is ϕ. Accordingly, in the case of antiparallel magnetization, the tunneling probability of the major-spin electrons is low even though the same biases V_{DS} and V_{GS} as those in the example case shown in FIG. **3**B are applied, and drain current is hardly generated. As the barrier height of the ferromagnetic tunnel barrier **7** in relation to the minor-spin electrons of the ferromagnetic source **3** is ϕ, the tunneling probability in relation to the minor-spin electrons is high. However, since the carrier density of the minor-spin electrons is low, the drain current generated by the tunneling of the minor-spin electrons is low. Accordingly, the drain current is also equal to the total current generated by the major-spin electrons and the minor-spin electrons of the ferromagnetic source in the case of antiparallel magnetization. However, the total current is lower than the total current obtained in the case of parallel magnetization. For this reason, the mutual (trans) conductance in the case of antiparallel magnetization is low.

Referring now to FIG. **4**, the current-voltage characteristics of the transistors shown in FIG. **1** through FIG. **3**C are described. FIG. **4** conceptually shows the V_{DS} dependence of the drain current I_D of the transistor **1** having V_{GS} as a parameter. In the case where the ferromagnetic source **3** and the ferromagnetic tunnel barrier **7** exhibit parallel magnetization, the bias V_{GS} that generates a predetermined drain current is set as $V_{\uparrow}$. In the case of parallel magnetization, $V_{GS}=V_{\uparrow}$ that is greater than $V_{\uparrow}$ (>$V_{\uparrow}$) is applied to the gate electrode, a drain current ($I_{D\uparrow\uparrow}$) **35** is generated by the tunneling of the major-spin electrons of the ferromagnetic source **3**, since the barrier height of the tunnel barrier in relation to the major-spin electrons of the ferromagnetic source is low as described above, and the effective width of the tunnel barrier is reduced by the gate voltage. As the effective width of the tunnel barrier can be controlled by adjusting the size of V_{GS}, the drain current **35** can be controlled also by adjusting V_{GS}.

If changes in the potential shape in the vicinity of the interface between the ferromagnetic source and the ferromagnetic tunnel barrier are caused by changes in the electric field mainly due to the gate voltage when V_{GS} is applied, the tunneling probability hardly depends on V_{DS}, and the drain current exhibits saturation characteristics with respect to V_{DS}, as shown in FIG. **4**.

Meanwhile, in the case where the ferromagnetic source and the ferromagnetic tunnel barrier exhibit antiparallel magnetization, the barrier height of the tunnel barrier in relation to the major-spin electrons of the ferromagnetic source is high ($\phi+\Delta$), and the tunneling probability is low. The barrier height in relation to the minor-spin electrons is low (ϕ), and the tunneling probability is high, but the carrier density is low. Accordingly, in the case of antiparallel magnetization, a drain current ($I_{D\downarrow\uparrow}$) **33** that is lower than the drain current in the case of parallel magnetization is generated even if V_{GS} is equal to V**1** (>$V_{\uparrow}$).

The above described transistor has such characteristics that a drain current can be controlled with a gate voltage. Also, the mutual conductance is high in the case where the relative magnetization between the ferromagnetic source **3** and the ferromagnetic tunnel barrier **7** is parallel magnetization, and the mutual conductance is low in the case where the relative magnetization is antiparallel magnetization.

A ferromagnetic structure can maintain magnetization directions unless a magnetic field greater than its coercive force is induced externally. Accordingly, the above described transistor can store binary information in a non-volatile manner by switching the relative magnetization of the ferromagnetic source **3** and the ferromagnetic tunnel barrier **7** between parallel magnetization and antiparallel magnetization. For example, the coercive force of the ferromagnetic source **3** and the coercive force of the ferromagnetic tunnel barrier **7** are made different from each other, or the magnetization direction of either the ferromagnetic source **3** or the ferromagnetic tunnel barrier **7** is fixed, so that the information of "0" can be stored by setting parallel magnetization between the ferromagnetic source **3** and the ferromagnetic tunnel barrier **7** using a magnetic field or the like generated by a signal line, and the information of "1" can be stored by setting antiparallel magnetization. As described above, this transistor can electrically detect the relative magnetization between the ferromagnetic source **3** and the ferromagnetic tunnel barrier **7**, based on the size of the drain current or the size of the mutual (trans) conductance. Accordingly, a one-bit non-volatile memory cell can be formed with the above described transistor alone.

FIG. **5** is a cross-sectional view illustrating an example structure of a transistor in accordance with a second embodiment of the present invention. As shown in FIG. **5**, the transistor **51** in accordance with this embodiment includes a tunnel junction structure and a control electrode structure. The tunnel junction structure has a ferromagnetic tunnel barrier **57** sandwiched between a ferromagnetic source **53** and a ferromagnetic drain **55**. The control electrode structure that includes a gate insulating film **61** and a gate electrode that are formed in relation to the ferromagnetic tunnel barrier **57**, and can induce en electric field in the ferromagnetic tunnel barrier **57**. The tunnel junction structure and the control electrode structure constitute the transistor **51**.

An electrically conductive ferromagnetic material such as a ferromagnetic metal and a ferromagnetic semiconductor with electric conductivity are employed for the ferromagnetic source **53** and the ferromagnetic drain **55**. An insulating ferromagnetic material such as an insulating ferromagnetic semiconductor is employed for the ferromagnetic tunnel barrier **57**. However, if ferromagnetic semiconductors are employed as the ferromagnetic source and the ferromagnetic drain, those two ferromagnetic semiconductors need to have the same conductivity. Specific examples of the materials are the same as those in the first embodiment.

Also, as in the first embodiment, in a case where a ferromagnetic metal or an n-type ferromagnetic semiconductor is employed for the ferromagnetic source **53**, the conduction carriers serve as electrons, and the bottom of the conduction band of the ferromagnetic tunnel barrier need to be spin-split. In a case where a p-type ferromagnetic semiconductor is used as the ferromagnetic source **53**, the conduction carriers serve as holes, and the top of the valence band of the ferromagnetic tunnel barrier **57** needs to be spin-split.

In the band structure in accordance with the second embodiment, the drain that is the same as the drain of the band structure shown in FIG. **2** should be made of a ferromagnetic material. In the second embodiment, Δ and ϕ can be determined in the same manner as in the first embodiment. If the direction of the major spin in the ferromagnetic source **53** is the same as the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier **57**, the magnetization configuration is parallel. If the spin directions are opposite to each other, the magnetization configuration is antiparallel. The magnetization of the ferromagnetic drain **55** may be the same as the magnetization of either the pin layer or the free layer (i.e., either the ferromagnetic source or the ferromagnetic tunnel barrier).

Especially in the transistor in accordance with the second embodiment, the ferromagnetic source **53** and the ferromagnetic drain **55** can be made of the same material, and accordingly, the process of manufacturing the transistor can be greatly simplified.

Next, a tunnel transistor in accordance with a third embodiment of the present invention is described. The transistor in accordance with this embodiment differs from the transistor of the first embodiment in that the ferromagnetic source is made of a half-metal ferromagnetic material (hereinafter referred to as "half metal"). A half metal exhibits a metallic band structure for one direction of spins, while exhibiting an insulating (or semi-conductive) spin band structure for the opposite direction of spins. Accordingly, the carriers of one direction serve as conduction carriers. If the spin direction of the conduction carriers (the spin direction of the carriers in the metallic spin band) in the half metal is the same as the spin direction of the spin band at the band edge of the ferromagnetic tunnel barrier, the magnetization configuration is parallel. It the spin directions are opposite to each other, the magnetization configuration is antiparallel. In the case of parallel magnetization, the spins belonging to the metallic spin band of the ferromagnetic source pass through the tunnel barrier of ϕ in height, and then generate a drain current. In the case of antiparallel magnetization, there are no conduction carriers with spins of ϕ in barrier height, because the ferromagnetic source is made of a half metal (with a ferromagnetic source made of a ferromagnetic metal described above, the conduction carriers are minor-spin electrons). As long as the band gap of the insulating spin band of the half metal is sufficiently wide and the half metal is sufficiently thick, carrier injection with such spins that can tunnel the ferromagnetic tunnel barrier from an external non-magnetic contact is hardly caused. Since the barrier height of the ferromagnetic tunnel barrier is $\phi+\Delta$ in relation to the spins belonging to the metallic spin band of the half metal, the tunnel probability in relation to the spins is low, and the drain current generated by the conduction carriers can be made so small as to be ignored if Δ is sufficiently large. In view of the above facts, with the ferromagnetic source made of a half metal, the difference in drain current between parallel magnetization and antiparallel magnetization can be made dramatically large. It is also possible to form both the ferromagnetic source and the ferromagnetic drain with half metals, as in the transistor in accordance with the second embodiment. Examples of half metals include CrO_2, Fe_3O_4, and Heusler's alloy. Also, ferromagnetic semiconductors with zinc blendestructures such as MnAs, CrAs, and CrSb, and ferromagnetic semiconductors with electronic structures that serve as half metals may be employed.

Next, a transistor in accordance with a fourth embodiment of the present invention is described in conjunction with FIG. **6**. FIG. **6** is a cross-sectional view illustrating the structure of the transistor in accordance with the fourth embodiment of the present invention. While the transistors in accordance with the first through third embodiments are planar transistors, the transistor in accordance with the fourth embodiment is formed by turning a transistor of any of the foregoing embodiments into a vertical transistor.

As shown in FIG. **6**, the transistor **71** in accordance with this embodiment is a stacked structure that includes a substrate **70**, a ferromagnetic source **73** formed on the substrate **70**, a ferromagnetic tunnel barrier **77**, and a ferromagnetic or non-magnetic drain **75**. The side surfaces of the components of the stacked structure are partially or entirely covered with a gate insulating film **81**. The transistor **71** further includes the gate insulating film **81** and a gate electrode **85** that can apply an electric field to the ferromagnetic tunnel bather **77** via the gate insulating film **81**.

As this structure is a stacked structure of the ferromagnetic source **73**, the ferromagnetic tunnel barrier **77**, and the ferromagnetic or non-magnetic drain **75** stacked in the normal direction of the surface of the substrate **70**, a series of junctions among the ferromagnetic source **73**, the ferromagnetic tunnel barrier **77**, and the ferromagnetic or non-magnetic drain **75** can be formed by a thin-film growth method with excellent controllability on film thickness. Accordingly, the ferromagnetic tunnel barrier **77** can be formed with high precision.

In each of the transistors of the first through fourth embodiments, a non-magnetic material may be interposed between the ferromagnetic source and the ferromagnetic tunnel barrier, so as to prevent magnetic coupling between the ferromagnetic source and the ferromagnetic tunnel barrier.

Next, memory circuits (a non-volatile memory) each having transistors of one of the first through fourth embodiments as a memory element, and the operations of such memory circuits are described in conjunction with the accompanying drawings.

The transistor of any of the first through fourth embodiments of the present invention is a transistor that can control the drain current by adjusting the gate voltage as in a case of a field-effect transistor such as a MOS transistor, and also has transfer characteristics (mutual conductance) that depend on the magnetization configuration of the ferromagnetic members that can hold magnetization information in the transistor in a non-volatile manner. Accordingly, the transistor alone can form a 1-bit memory cell. Also, the output voltage of the transistor can be arbitrarily set in accordance with the peripheral circuits (loads and the power source).

FIGS. 7A and 7B illustrate memory circuits in accordance with fifth and sixth embodiments of the present invention. These memory circuits each have one of transistors in accordance with one of the first through fourth embodiments of the present invention. As shown in FIG. 7A, a memory circuit in accordance with this embodiment has a number of transistors **91** that have sources (S) grounded, and are arranged in a matrix fashion. The drain (D) and the gate (G) of each of the transistor **91** are connected to a read bit line BL and a read word line WL, respectively. Also, each rewrite word line crosses each rewrite bit line on the transistor, with each rewrite word line and each rewrite bit line being electrically insulated from other lines. The read bit lines and the read word lines may also serve as the rewrite word lines and the rewrite bit lines. FIGS. 7A and 7B shows such cell structures. In each of the structure, a memory cell can be formed with a single transistor, and the lines can have very simple structures.

Next, the fifth embodiment of the present invention is described in greater detail, with reference to the accompanying drawings. A conventional MRAM has a 2-element, 4-line structure (see FIG. **8**). In such a MRAM, it is difficult to reduce the cell area by sharing a source between adjacent cells, for example, due to the existence of MTJs and rewrite word lines. In this embodiment, on the other hand, each memory cell can be formed with a 1-element, 3-line structure (or a 1-element, 2-line structure) that is the simplest structure, as shown in FIG. 7A. Accordingly, a layout that is suitable for a miniaturization can be easily realized. For example, a source is shared to further reduce the size of each memory cell (later described).

In the following, the read bit lines and the read word lines also serve as the rewrite bit lines and the rewrite word lines, and the read/rewrite bit lines are referred to as bit lines BL while the read/rewrite word lines are referred to as word lines WL. Information is rewritten by varying the coercive force of the ferromagnetic source or the ferromagnetic tunnel barrier of each transistor **91** of this embodiment, or by switching the relative magnetization between the ferromagnetic source and the ferromagnetic tunnel barrier to parallel magnetization or antiparallel magnetization, with the magnetization direction of either one of the ferromagnetic source and the ferromagnetic tunnel barrier being fixed while the magnetization of the other being inverted. The magnetization configurations of parallel magnetization and antiparallel magnetization are represented by binary information of “0” and “1”. More specifically, currents are applied to the bit line BL and the word line WL crossing each other on a selected cell, and the magnetization of the ferromagnetic member having the smaller coercive force or the ferromagnetic member having an unfixed magnetization direction in the selected memory cell is inverted by the composite magnetic field of the magnetic fields induced by the currents. Thus, information is stored.

The value of the current to be applied to each line is set so as not to cause magnetization inversion with the magnetic field generated only from one of the lines. By doing so, the unselected memory cells connected to the bit line BL and the word line WL to which the selected memory cell is connected are protected from magnetization inversion.

The information is read out by detecting the size of the drain current. The drain current detection is carried out by applying a voltage to the word line WL connected to the selected cell to energize the transistor of this embodiment, and then applying a voltage to the bit line BL. In the transistor of this embodiment, the mutual conductance is high and a high drain current is generated, when the relative magnetization configuration between the ferromagnetic source and the ferromagnetic tunnel barrier is parallel magnetization. In the case of antiparallel magnetization, however, the mutual conductance is low, and the drain current is also low. Accordingly, the relative magnetization configuration between the ferromagnetic source and the ferromagnetic tunnel barrier can be detected.

With a regular MTJ, the current is generated by the tunneling between the state densities of the major-spin electrons and the minor-spin electrons of both ferromagnetic electrodes in the parallel magnetization configuration. In the case of antiparallel magnetization, the current is generated by the tunneling from the state density of the minor-spin electrons to the state density of the major-spin electrons and the tunneling from the state density of the major-spin electrons to the state density of the minor-spin electrons. Accordingly, the current ratio between the parallel magnetization configuration and the antiparallel magnetization configuration becomes higher, as the spin polarization rate of the ferromagnetic electrodes becomes higher. However, since the current generated in the case of parallel magnetization contains current components generated by the minor-spin electrons, the current ratio between the parallel magnetization configuration and the antiparallel magnetization configuration cannot be easily made higher.

In the transistor in accordance with this embodiment, on the other hand, the drain current is generated only by the tunneling of the major-spin electrons of the ferromagnetic source in the case of parallel magnetization, because the band edge of the ferromagnetic tunnel barrier is spin-split. In the case of antiparallel magnetization, the drain current is generated only by the tunneling of the minor-spin electrons of the ferromagnetic source. Also, the ferromagnetic tunnel barrier exhibits high spin selectivity. Accordingly, in the transistor in accordance with this embodiment, the current ratio (the drain current ratio) between the parallel magnetization configuration and the antiparallel magnetization configuration can be made higher than the current ratio in the case with a MTJ. Thus, with the transistor in accordance with this embodiment, the magnetization configuration can be easily detected in the circuit.

In a conventional MTJ, the TMR ratio rapidly decreases when the bias voltage drops. As a result, the TMR ratio greatly decreases with the bias necessary for the circuit. With the transistor in accordance with this embodiment, such a problem is not caused. As the tunneling effect that depends on the spin direction due to FN tunneling is utilized in the transistor in accordance with this embodiment, the bias required for generating the FN tunneling can be adjusted with the barrier height or the film thickness of the tunnel barrier. Accordingly, a high drain current ratio can be achieved with the bias required for the circuit.

The tunnel structure that has the ferromagnetic tunnel barrier interposed between the ferromagnetic source and the ferromagnetic or non-magnetic drain (the two-terminal device of the transistor of any of the first through fourth embodiments minus the gate insulator and the gate electrode) may also be used as a two-terminal magnetoresistive device that can optimize the bias voltage to achieve a high TMR ratio.

Next, the sixth embodiment of the present invention is described, with reference to the accompanying drawings. FIG. 7B illustrates a memory circuit that is the same as the memory circuit of FIG. 7A, except that the end of the bit line BL is connected to an output terminal V_O and to a power supply V_{DD} via a load branching out from the output terminal V_O. FIG. 7C shows the output characteristics of the memory circuit shown in FIG. 7B. Although an active load formed

with a depletion MOS transistor is employed as the load in the memory circuit shown in FIG. **7**B, a pure resistance may also be employed. As shown in FIG. **7**C, as a bias V_{GS} is applied to the gate electrode of the transistor and the supply voltage V_{DD} is applied to the bit line BL via the load at the time of reading information, the operating point (P**11** and P**12** in FIG. **7**C) due to the load moves on the load curve in accordance with the magnetization configuration between the ferromagnetic source and the ferromagnetic tunnel barrier. Accordingly, the output signals V_O are represented by $V_{o\uparrow\uparrow}$ and $V_{O\downarrow\uparrow}$ in FIG. **7**C. The absolute values of the output signals and the ratio ($V_{O\uparrow\uparrow}/V_{O\downarrow\uparrow}$) can be made appropriate by the peripheral circuits such as the load and the power supply V_{DD}. For example, a high output signal ratio can be obtained by optimizing the load curve even if the drain current ratio $I_{D\uparrow\uparrow}/I_{D\downarrow\uparrow}$ on is low. Also, even if the values of $I_{D\uparrow\uparrow}$ and $I_{D\downarrow\uparrow}$ vary among the memory cells, the output voltage hardly varies, as long as the saturation current of the active load is higher than $I_{D\downarrow\uparrow}$ and is lower than $I_{D\uparrow\uparrow}$. Since a sense amplifier is not used for reading information, high-speed reading can be performed. Accordingly, the memory circuit in accordance with this embodiment is advantageous in that an output signal of a desired size can be easily obtained, and high-speed reading can be performed.

It is also possible to form a memory cell structure that is suitable for high-density integration, having one source shared between two transistors of any of the first through third embodiments. FIG. **9** is a cross-sectional view illustrating an example of such a memory cell having a shared source. The memory cell structure shown in FIG. **9** includes: a first transistor Tr**1** and a second transistor Tr**2** that are the two transistors adjacent to each other; a word line WL to which the gate electrode G**1** of the first transistor Tr**1** and the gate electrode G**2** of the second transistor Tr**2** are connected; a first bit line BL**1** to which the drain D**1** of the first transistor Tr**1** is connected; a second bit line BL**2** to which the drain D**2** of the second transistor Tr**2** is connected; a ferromagnetic source S that is shared between the first transistor Tr**1** and the second transistor Tr**2**; and a line (GND) that grounds the ferromagnetic source S. Memory cells each having this structure are arranged in a matrix fashion to achieve higher-density integration.

FIG. **10** is a cross-sectional view illustrating a memory cell structure in which transistors of the fourth embodiment (see FIG. **6**) are employed. In this structure, the ferromagnetic sources S of the transistors that are arranged in a matrix fashion on a substrate or on a contact layer formed on the substrate are connected to one another and are grounded (GND). The transistors aligned in the row direction are connected to one another with the bit line that collectively connects the drains D of the transistors. The transistors aligned in the column direction are connected to one another with the word line that collectively connects the gate electrodes G of the transistors. With this structure, the integration density can be further increased.

Transistors each having a ferromagnetic tunnel barrier, a ferromagnetic source made of a ferromagnetic metal, a ferromagnetic semiconductor, or a half metal, and a ferromagnetic drain made of a ferromagnetic metal, a ferromagnetic semiconductor, or a half metal, have been described so far. However, the same effects can be achieved by forming a transistor that includes a ferromagnetic tunnel barrier, a source made of a non-magnetic conductor, and a ferromagnetic drain made of a ferromagnetic metal, a ferromagnetic semiconductor, or a half metal.

In a case of such a transistor that includes a non-magnetic source, a ferromagnetic tunnel barrier, and a ferromagnetic drain, the current ratio between the parallel magnetization configuration and the antiparallel magnetization configuration might be decreased by the bias between the source and the drain.

In the following, transistors based on the second aspect of the present invention and the application of the transistors to non-volatile memories are described. Each of the transistors is a metal-insulator-semiconductor field-effect transistor (MISFET) that has a ferromagnetic semiconductor serving as a channel region. A source and a drain are each designed to include a tunnel barrier joined to the ferromagnetic semiconductor layer as the channel region, and an electrode joined to the tunnel barrier. At least either one of the source and the drain includes a ferromagnetic material. Hereinafter, a source and a drain containing a ferromagnetic material will be referred to as a ferromagnetic source and a ferromagnetic drain, and a source and a drain made of a non-magnetic material will be referred to as a non-magnetic source and a non-magnetic drain. The ferromagnetic source and the ferromagnetic drain are each designed to include a tunnel barrier made of a non-magnetic material (a non-magnetic tunnel barrier) and an electrode made of a ferromagnetic material (a ferromagnetic electrode). Alternatively, the ferromagnetic source and the ferromagnetic drain may be each designed to include a tunnel barrier made of a ferromagnetic material (a ferromagnetic tunnel barrier) and an electrode made of a non-magnetic material (a non-magnetic electrode). These MISFETs can be roughly classified into seventh through ninth embodiments of the present invention, according to the structure of the ferromagnetic source and the ferromagnetic drain ((1) through (3) below).

(1) Ferromagnetic Electrode/Non-magnetic Tunnel Barrier Structure

FIG. **11**A illustrates the structure of a MISFET in accordance with the seventh embodiment of the present invention. As shown in FIG. **11**A, the MISFET in accordance with the seventh embodiment includes a MIS structure, a ferromagnetic source **203**, and a non-magnetic drain **205**. The MIS structure includes a gate electrode **215**, a gate insulating film **211**, and a ferromagnetic semiconductor layer **207** (in spite of the ferromagnetic semiconductor, this stacked structure is referred to as a MIS structure as in the case of a metal-insulator-semiconductor structure). The ferromagnetic source **203** includes a non-magnetic tunnel barrier **203***b* joined to the ferromagnetic semiconductor layer **207**, and a ferromagnetic electrode **203***a* joined to the non-magnetic tunnel barrier **203***b*. The non-magnetic drain **205** includes a non-magnetic tunnel barrier **205***b* joined to the ferromagnetic semiconductor layer **207**, and a non-magnetic electrode **205***a* joined to the non-magnetic tunnel barrier **205***b*. Although the combination of a ferromagnetic source and a non-magnetic drain is shown in FIG. **11**A, it is also possible to form a ferromagnetic drain with a non-magnetic tunnel barrier and a ferromagnetic electrode, and a non-magnetic source with a non-magnetic tunnel barrier and a non-magnetic electrode. Alternatively, the source and the drain may be a ferromagnetic source and a ferromagnetic drain.

The ferromagnetic semiconductor layer **207** that forms the channel region is formed with a ferromagnetic semiconductor that contains magnetic elements at high concentration in the semiconductor as the base material. The ferromagnetic semiconductor layer **207** is formed through growth on a semiconductor substrate or a semiconductor layer (not shown), or by introducing magnetic atoms into the semiconductor through thermal diffusion or ion implantation. Alternatively, the ferromagnetic semiconductor layer **207** may be doped with magnetic elements so as to cause degeneracy, or so as not to

cause degeneracy. Specific examples of the materials for the ferromagnetic semiconductor layer **207** include $Si_{1-x}M_x$, $Ge_{1-x}M_x$, $(SiGe)_{1-x}M_x$ (M being magnetic elements), which are ferromagnetic semiconductors doped with magnetic elements in semiconductors such as Si and Ge at high concentration. Examples of the materials for the ferromagnetic electrode to be the ferromagnetic source or the ferromagnetic drain (or both) include regular ferromagnetic metals (such as Fe, Ni, Permalloy, CoFe alloy, and CoFeB alloy), ferromagnetic semiconductors doped with magnetic elements at high concentration (such as $Si_{i-x}M_x$, $Ge_{1-x}M_x$, $(SiGe)_{1-x}M_x$ (M being magnetic elements), and half-metal ferromagnetic materials (such as magnetite, Heusler's alloy, CrO_2, and MnAs, CrAs, and MnSb having zinc blendestructures). The ferromagnetic electrodes used for the ferromagnetic source and the ferromagnetic drain may be grown or deposited on the ferromagnetic semiconductor layer **207**, but may also be formed by introducing magnetic atoms into the semiconductor through thermal diffusion or ion implantation. So as to form a non-magnetic electrode, it is possible to use a non-magnetic metal (such as Al, PdSi alloy, or ErSi alloy), or a conduction-controlled non-magnetic semiconductor (such as Si, Ge, or SiGe alloy). As for the non-magnetic tunnel barriers, a non-magnetic insulator (such as a Si oxide, a Si nitride, an Al oxide, or a Ta oxide) or a non-magnetic semiconductor such as SiC can be employed. The MIS structure can be formed with a MOS structure in which the surface of the ferromagnetic semiconductor layer is oxidized, or with a structure produced by growing or depositing the insulating layer (such as a Si oxide, an Al oxide, or Hf oxide) **211** on the ferromagnetic semiconductor layer **207**. The substrate is a regular semiconductor substrate or a SOI substrate. The MISFET **201** in accordance with this embodiment is of an accumulation channel type, with the conduction carriers being of the same conductivity type as the ferromagnetic semiconductor layer **207** serving as the channel region. Although the carriers may be either electrons or holes, the energy band structure in a case of an n-channel device will be described in the following. However, the same structure can be employed for a p-channel device.

FIGS. **11**B through **11**D illustrate examples of the band structures in the vicinity of the channel region when the MISFET in accordance with the seventh embodiment of the present invention is in a thermal equilibrium state. Here, each ferromagnetic electrode is made of a ferromagnetic metal, and each non-magnetic electrode is made of a non-magnetic metal. The structure shown in FIG. **11**B includes a ferromagnetic source **203-1** that is formed with a ferromagnetic electrode **203***a***-1** and a non-magnetic tunnel barrier **203***b***-1**, and a non-magnetic drain **205-1** that is formed with a non-magnetic electrode **205***a***-1** and a non-magnetic tunnel barrier **205***b***-1**. The structure shown in FIG. **11**C includes a non-magnetic source **203-2** that is formed with a non-magnetic electrode **203***a***-2** and a non-magnetic tunnel barrier **203***b***-2**, and a ferromagnetic drain **205-2** that is formed with a ferromagnetic electrode **205***a***-2** and a non-magnetic tunnel barrier **205***b***-2**. The structure shown in FIG. **11**D includes a ferromagnetic source **203-3** that is formed with a ferromagnetic electrode **203***a***-3** and a non-magnetic tunnel barrier **203***b***-3**, and a ferromagnetic drain **205-3** that is formed with a ferromagnetic electrode **205***a***-3** and a non-magnetic tunnel barrier **205***b***-3**. For ease of explanation, each structure is in a flat band state at the time of thermal equilibrium. The solid lines shown on the ferromagnetic source **203** and the ferromagnetic drain **205**, and the dotted line shown across the ferromagnetic semiconductor layer **207** and the non-magnetic tunnel barriers **203***b* and **205***b* indicate the Fermi energy E_F. The band gap of the ferromagnetic semiconductor is denoted by E_G. The bottom of the conduction band and the top of the valence band of the semiconductor are denoted by E_C and E_V, respectively. Hereinafter, E_F, E_G, E_C, and E_Y represent the same as above. Although the ferromagnetic semiconductor layer **207** as the channel region is not degenerated in FIGS. **11**B through **11**D, the ferromagnetic semiconductor layer **207** may be doped with magnetic elements at such concentration as to cause degeneracy, as described above. In an n-channel device, the non-magnetic tunnel barriers of the source and the drain are designed to form energy barriers of ϕ_s and ϕ_D in height when seen from the ferromagnetic (or non-magnetic) electrode of the source and the ferromagnetic (or non-magnetic) electrode of the drain. Those energy barriers are formed at least on the side of the conduction band. In a p-channel device, energy barriers are formed at least on the valence band side.

The arrows shown over the Fermi energy E_F of the ferromagnetic electrode **203***a* and the non-magnetic electrode **205***a* indicate the directions of the major-spin electrons in the respective regions. Each upward-pointing arrow represents the up-spin direction, and each downward-pointing arrow represents the down-spin direction. The minor-spin electrons are not shown. Likewise, the arrow shown over the E_C of the ferromagnetic semiconductor layer indicates the direction of the major spin. The non-magnetic electrode is represented by showing both an upward-pointing arrow and a downward-pointing arrow. In the following descriptions, those arrows shown in FIGS. **11**B through **11**D will be used to the same effects as above.

(2) Ferromagnetic Electrode/Intrinsic Semiconductor Tunnel Barrier

FIG. **12**A illustrates the device structure of a MISFET in accordance with an eighth embodiment of the present invention. The MISFET in accordance with the eighth embodiment of the present invention differs from the MISFET in accordance with the seventh embodiment of the present invention in that the non-magnetic tunnel barriers **203***b* and **205***b* are replaced with intrinsic semiconductors (or semiconductors moderately doped with impurities). As in the MISFET in accordance with the seventh embodiment of the present invention, a ferromagnetic electrode is used for at least either one of the source and the drain. The structure shown in FIG. **12**A has a ferromagnetic source and a non-magnetic drain. The structures and materials of the ferromagnetic semiconductor layer as the channel region, the ferromagnetic electrode, the non-magnetic electrode, and the substrate are the same as those of the MISFET in accordance with the seventh embodiment of the present invention. The non-magnetic tunnel barriers **223***b* and **225***b* may be formed with semiconductors that serve as host materials for the ferromagnetic semiconductor layer **227** used as the channel region. For example, if the ferromagnetic semiconductor layer as the channel region is formed with $Si_{1-x}M_x$ (M being magnetic elements), the non-magnetic tunnel barriers are formed with non-doped Si (or semiconductors moderately doped with impurities).

The MISFET in accordance with the eighth embodiment of the present invention also operates as an accumulate channel type, and the carriers may be either electrons or holes. However, the band structures in n-channel devices will be described in the following. The same structures can be used for p-channel devices.

FIGS. **12**B through **12**D illustrate the band structures in the vicinity of the channel region when the MISFET in accordance with the eighth embodiment of the present invention is in a thermal equilibrium state. Here, each ferromagnetic electrode is made of a ferromagnetic metal, and each non-magnetic electrode is made of a non-magnetic metal. The struc-

ture shown in FIG. **12**B includes a ferromagnetic source **223-1** that is formed with a ferromagnetic electrode **223***a***-1** and a non-magnetic tunnel barrier **223***b***-1**, and a non-magnetic drain **225-1** that is formed with a non-magnetic electrode **225***a***-1** and a non-magnetic tunnel barrier **225***b***-1**. The structure shown in FIG. **12**C includes a non-magnetic source **223-2** that is formed with a non-magnetic electrode **223***a***-2** and a non-magnetic tunnel barrier **223***b***-2**, and a ferromagnetic drain **225-2** that is formed with a ferromagnetic electrode **225***a***-2** and a non-magnetic tunnel barrier **225***b***-2**. The structure shown in FIG. **12**D includes a ferromagnetic source **223-3** that is formed with a ferromagnetic electrode **223***a***-3** and a non-magnetic tunnel barrier **223***b***-3**, and a ferromagnetic drain **225-3** that is formed with a ferromagnetic electrode **225***a***-3** and a non-magnetic tunnel barrier **225***b***-3**. In an n-channel device, the barriers shown in the drawings are formed with the intrinsic semiconductors of the source and the drain (however, the gap in potential caused on the interface between the ferromagnetic semiconductor layer and each intrinsic semiconductor layer is not shown), so that energy barriers of ϕ_s and ϕ_D in height can be formed on the side of the conduction band. In a p-channel device, energy barriers are formed on the valence band side.

(3) Non-magnetic Electrode/Ferromagnetic Tunnel Barrier

FIG. **13**A illustrates the device structure of a MISFET in accordance with a ninth embodiment of the present invention. The MISFET in accordance with the ninth embodiment of the present invention differs from the MISFET in accordance with the seventh embodiment of the present invention in that the non-magnetic tunnel barriers **203***b* and **205***b* (FIG. **11**A) are replaced with a ferromagnetic tunnel barrier **243***b* and a non-magnetic tunnel barrier **245***b*, and the ferromagnetic electrode **203***a* and the non-magnetic electrode **205***a* (FIG. **11**A) are replaced with non-magnetic electrodes **243***a* and **245***a*. Although the source and the drain in the structure shown in FIG. **13**A are a ferromagnetic source and a non-magnetic drain, a ferromagnetic tunnel barrier should be employed in at least either one of the source and the drain. If a ferromagnetic tunnel barrier is employed in only either one of the source and the drain, a non-magnetic tunnel barrier is employed in the other one of the source and the drain. The structures and materials of the ferromagnetic semiconductor layer **247** as the channel region, the non-magnetic electrodes **243***a* and **245***a*, and the substrate are the same as those of the MISFET in accordance with the seventh embodiment of the present invention. The ferromagnetic tunnel barrier **243***b* may be formed with an insulating ferromagnetic material or an insulating ferromagnetic semiconductor. Specific examples of the materials for the ferromagnetic tunnel barrier **243***b* include EuS and Gd_2O_3. The MISFET in accordance with the ninth embodiment of the present invention also operates as an accumulate channel type, and the carriers may be either electrons or holes. However, the band structures in n-channel devices will be described in the following. The same structures can be employed for p-channel devices.

FIGS. **13**B through **13**D illustrate the band structures in the vicinity of the channel region when the third device structure is in a thermal equilibrium state. Here, each ferromagnetic electrode is made of a ferromagnetic metal, and each non-magnetic electrode is made of a non-magnetic metal. The structure shown in FIG. **13**B includes a ferromagnetic source **243-1** that is formed with a non-magnetic electrode **243***a***-1** and a ferromagnetic tunnel barrier **243***b***-1**, and a non-magnetic drain **245-1** that is formed with a non-magnetic electrode **245***a***-1** and a non-magnetic tunnel barrier **245***b***-1**. The structure shown in FIG. **13**C includes a non-magnetic source **243-2** that is formed with a non-magnetic electrode **243***a***-2** and a non-magnetic tunnel barrier **243***b***-2**, and a ferromagnetic drain **245-2** that is formed with a non-magnetic electrode **245***a***-2** and a ferromagnetic tunnel barrier **245***b***-2**. The structure shown in FIG. **13**D includes a ferromagnetic source **243-3** that is formed with a non-magnetic electrode **243***a***-3** and a ferromagnetic tunnel barrier **243***b***-3**, and a ferromagnetic drain **245-3** that is formed with a non-magnetic electrode **245***a***-3** and a ferromagnetic tunnel barrier **245***b***-3**. At the band edges of the ferromagnetic tunnel barriers **243***b***-1**, **245***b***-2**, **243***b***-3**, and **245***b***-3**, the barrier height seen from each adjacent non-magnetic electrode depends on the spins, because of the spin split in the up-spin band and the down-spin band. In an n-channel device, the bottom of the conduction band of each ferromagnetic tunnel bather needs to be spin-split. In a p-channel device, the top of the valence band of each ferromagnetic tunnel barrier needs to be spin-split. The two adjacent solid lines in each ferromagnetic tunnel barrier in the drawings indicate the band edges of the up-spin band and the down-spin band, and Δ_S and Δ_D indicate the spin-split width in the up-spin band and the down-spin band in each ferromagnetic tunnel barrier in the case where a ferromagnetic tunnel barrier is employed for the source and the drain. Each upward-pointing arrow and each downward-pointing arrow shown over the solid lines indicate an up-spin band edge and a down-spin band edge. The barrier height of the lower ferromagnetic tunnel barrier or the non-magnetic tunnel barrier seen from the non-magnetic electrode of the source is denoted by ϕ_s in the source, and the barrier height of the lower ferromagnetic tunnel barrier or the non-magnetic tunnel barrier seen from the non-magnetic electrode of the drain is denoted by ϕ_D in the drain.

The above described structures are the basic structures of the MISFETs in accordance with the seventh through ninth embodiments of the present invention. Each of the basic structures can be embodied by the specific structures illustrated in FIGS. **14**A through **14**D. The electrodes and the tunnel barriers of the sources and the drains shown in FIGS. **14**A through **14**D are formed with ferromagnetic materials, so that the MISFETs in accordance with the seventh through ninth embodiment of the present invention illustrated in FIGS. **11**A through **13**D can be embodied.

FIGS. **14**A through **14**D illustrate MISFETs in practical forms in accordance with tenth through thirteenth embodiments of the present invention. FIG. **14**A illustrates the structure of the MISFET in accordance with the tenth embodiment of the present invention. As shown in FIG. **14**A, the MISFET **300** in accordance with this embodiment includes a ferromagnetic semiconductor layer **307** that is formed in an island fashion on a substrate **301**, and a source and a drain formed with ferromagnetic (or non-magnetic) electrodes **303***a* and **305***a* that are separated from the ferromagnetic semiconductor layer **307** and the substrate **301** by ferromagnetic (or non-magnetic) tunnel barriers **303***b* and **305***b*.

FIG. **14**B illustrates a MISFET in a second practical form in accordance with the eleventh embodiment of the present invention. This is an example a three-layer structure of a ferromagnetic semiconductor layer, ferromagnetic (or non-magnetic) tunnel barriers, and ferromagnetic (or non-magnetic) electrodes. The MISFET **320** in accordance with this embodiment has a three-layer structure formed with a ferromagnetic semiconductor layer **327**, a ferromagnetic (or non-magnetic) tunnel barriers **323***b* and **325***b*, and a ferromagnetic (or non-magnetic) electrodes **323***a* and **325***a* arranged in this order on a substrate **321**. A concavity having a U-shape, V-shape, or the like in a section seen from one direction of the three-layer structure is formed in the three-layer structure by

a lithography technique or an etching technique. An insulating film **331** and a gate electrode **335** are formed on the surfaces of the ferromagnetic semiconductor, the ferromagnetic (or non-magnetic) tunnel barrier, and the ferromagnetic (or non-magnetic) electrode, which are exposed through the concavity.

FIG. **14**C illustrates a MISFET in a third practical form in accordance with the twelfth embodiment of the present invention. This MISFET is an example structure having an SOI substrate. As shown in FIG. **14**C, the MISFET **340** in accordance with this embodiment includes: an SOI structure that is formed with a substrate **341** and an embedded oxide film **342** formed on the substrate **341**; an island-like ferromagnetic semiconductor **347** formed on the SOI structure; a source and a drain that are formed with or non-magnetic tunnel barriers formed on the opposite side surfaces of the ferromagnetic semiconductor **347** and ferromagnetic (or non-magnetic) electrodes joined to the ferromagnetic (or non-magnetic) tunnel barriers; a gate insulating film **351** formed on the ferromagnetic semiconductor **347**; and a gate electrode **355** formed on the gate insulating film **351**. In the existence of the embedded oxide film **342**, the tunnel barriers **343***b* and **345***b* are formed only on the side walls of the ferromagnetic semiconductor **347**.

FIG. **14**D illustrates a MISFET in a fourth practical form in accordance with the thirteenth embodiment of the present invention. This MISFET is an example of a vertical transistor. As shown in FIG. **14**D, the MISFET in the fourth practical form includes an island-like stacked structure that is formed with a source **363**, a ferromagnetic semiconductor **367**, and a drain **365** formed on a substrate **361**. A gate insulating film **371** and a gate electrode **373** are formed on a side wall of the stacked structure.

Next, the operation principles of the MISFET in accordance with a second aspect of the present invention are described, with reference to the accompanying drawings. While the channel region in each of the MISFETs of the seventh through thirteenth embodiments of the present invention is formed with a ferromagnetic semiconductor layer, combinations of a source and a drain include: (i) a ferromagnetic source and a non-magnetic drain; (ii) a non-magnetic source and a ferromagnetic drain; (iii) a ferromagnetic source and a ferromagnetic drain, as described above. Each ferromagnetic source or drain is formed with: (a) junction of a ferromagnetic electrode and a non-magnetic tunnel barrier; (b) junction of a ferromagnetic electrode and an intrinsic semiconductor barrier; or (c) junction of a non-magnetic electrode and a ferromagnetic tunnel barrier.

In the following, the principles of operation are described as to an n-channel device that has a ferromagnetic source formed with the junction of a ferromagnetic electrode and a non-magnetic tunnel barrier or the junction of a non-magnetic electrode and a ferromagnetic tunnel barrier. The principles of operation of a MISFET having a ferromagnetic source formed with the junction of a ferromagnetic electrode and an intrinsic semiconductor barrier are the same as those in a case of the junction of a ferromagnetic electrode and a non-magnetic tunnel barrier. The same applied to a p-channel device. If the magnetization direction of the ferromagnetic channel region is the same as the magnetization direction of the ferromagnetic source, the relative magnetization configuration is parallel. If the magnetization direction of the ferromagnetic channel region is opposite to the magnetization direction of the ferromagnetic source, the relative magnetization configuration is antiparallel. In a case where ferromagnetic tunnel barriers are employed, if the direction of the major spin in the ferromagnetic semiconductor layer is parallel to the spin direction of the spin band forming the band edge in each ferromagnetic tunnel barrier, the relative magnetization configuration is parallel. If the direction of the major spin in the ferromagnetic semiconductor layer is opposite to the spin direction of the spin band forming the band edge in each ferromagnetic tunnel barrier, the relative magnetization configuration is antiparallel. Here, a Rashba effect that is induced by the gate voltage is ignored. The channel length is sufficiently shorter than the relaxation length of spins.

In the following, the operation principles of a MISFET in accordance with the seventh embodiment are described. FIGS. **15**A through **15**C illustrate the band structures of a MISFET having a ferromagnetic source **403** formed with a ferromagnetic electrode **403***a* and a non-magnetic tunnel barrier **403***b*. FIG. **15**A illustrates the band structure in a case where the gate-source bias V_{is} is set to zero, and a bias V_{GS} (>0) is applied between the drain and the source. As the bias V_{DS} is applied, the potential shown in FIG. **15**A is formed. Since the potential of the gate electrode located in the vicinity of the drain is set to zero, the decrease in the potential of the tunnel barrier of the drain is greater than the decrease in the potential of the tunnel barrier of the source. As long as the barrier width d of the tunnel barrier of the ferromagnetic source is suitably set, electrons are hardly injected into the channel region from the ferromagnetic source due to a tunneling effect. Although a current might be generated from the conduction carriers of the ferromagnetic electrode of the ferromagnetic source that thermally cross over the barrier of ϕ_S in height, the current can be restricted to a sufficiently small amount by adjusting the height ϕ_S to a suitable value. Accordingly, when the bias V_{GS} is zero, the MISFET is put into a shut-off state. This shut-off state does not depend on the relative magnetization direction between the ferromagnetic source and the ferromagnetic channel.

When a bias V_{GS} (>0) is applied to the gate electrode, the electric field in the vicinity of the tunnel barrier of the ferromagnetic source is intensified by the electric flux flowing from the gate electrode to the ferromagnetic source, and the barrier width of the tunnel barrier decreases as indicated by d' in FIG. **15**B. Accordingly, the potential barrier of ϕ_S transmits the electrons in the ferromagnetic source, and the electrons are injected into the channel region located immediately below the gate insulating film. While being drawn toward the interface between the insulator and the semiconductor by virtue of the bias V_{GS}, the injected electrons are transported to the drain by virtue of the bias V_{DS}, and then form a drain current. Here, the trans (mutual) conductance and the drain current of the MISFET **401** in accordance with this embodiment depends on the relative magnetization direction between the ferromagnetic source **403** and the ferromagnetic channel region **407**.

The electrons tunneling from the ferromagnetic source **403** to the ferromagnetic channel region **407** via a tunnel barrier have the same effect as a tunneling magneto-resistance (TMR) effect (hereinafter referred to simply as the TMR effect). Accordingly, the tunnel resistance is low in a case where the ferromagnetic source **403** and the ferromagnetic channel region **407** exhibit parallel magnetization, and the tunnel resistance is high in a case of antiparallel magnetization. Even if the influence of the TMR effect is small, electrons with a spin polarization rate that depends on the spin polarization rate of the ferromagnetic material of the source can be injected from the ferromagnetic source **403**. Accordingly, the electrons cause spin-dependent scattering in the ferromagnetic channel region **407**, in accordance with the relative magnetization configuration between the ferromagnetic channel region **407** and the ferromagnetic source **403**.

Due to the TMR effect and the spin-dependent scattering in the ferromagnetic channel region at the time of tunnel injection, the trans conductance varies in accordance with the relative magnetization direction between the ferromagnetic source **403** and the ferromagnetic channel region **407**.

As shown in FIG. **15**B, if the ferromagnetic source **403** and the ferromagnetic channel region **407** exhibit parallel magnetization, the trans conductance and the drain current become higher. As shown in FIG. **15**C, if the ferromagnetic source **403** and the ferromagnetic channel region **407** exhibit antiparallel magnetization, the trans conductance and the drain current become low.

As described above, in the MISFET in accordance with this embodiment, the trans conductance can be controlled by the relative magnetization direction between the ferromagnetic source **403** and the ferromagnetic channel region **407**, even with the same bias being applied. In the MISFET **401** in accordance with this embodiment, the number of carriers to be injected into the channel region can be controlled by the bias V_{GS}, and accordingly, the drain current can be controlled by the bias V_{GS}. In this manner, the MISFET in accordance with this embodiment has the characteristics of a regular transistor that can control the drain current with the gate voltage, and can also control the trans conductance in accordance with the relative magnetization direction between the ferromagnetic source **403** and the ferromagnetic channel region **407**. A MISFET having the tunnel barrier of the ferromagnetic source formed with an intrinsic semiconductor operates in the same manner as above.

Next, the operation principles of a MISFET in accordance with the ninth embodiment of the present invention are described. FIGS. **16**A through **16**C illustrate the band structures of a MISFET having a ferromagnetic source formed with a non-magnetic electrode and a ferromagnetic tunnel barrier joined to each other. FIG. **16**A illustrates the band structure in a case where the gate-source bias V_{GS} is set to zero, and a bias V_{DS} (>0) is applied. Since the potential of the gate electrode located in the vicinity of the drain is set to zero, the decrease in the potential of the tunnel barrier of the drain is greater than the decrease in the potential of the tunnel barrier of the source. Because of the spin split in the ferromagnetic tunnel barrier **435**b of the source, the barrier height varies with the directions of spin, when seen from the electrons of the non-magnetic electrode **423**a of the source. In the structure shown in FIG. **16**A, the barrier height is lower for the up-spin electrons than for the down-spin electrons in the non-magnetic electrode of the source. However, as long as the barrier width d of the tunnel barrier of the ferromagnetic source is suitably set, up-spin electrons are hardly injected into the channel region from the ferromagnetic source due to a tunneling effect even when the bias V_{DS} (>0) is applied, with V_{GS} being zero. Although a current might be generated from the carriers of the non-magnetic electrode **423**a of the ferromagnetic source that thermally cross over the ferromagnetic tunnel barrier **423**b, the current can be restricted to a sufficiently small amount by adjusting the barrier height ϕ_s to a suitable value. Accordingly, when the bias V_{GS} is zero, the MISFET is put into a shut-off state. This shut-off state is not affected by the relative magnetization direction between the ferromagnetic source **423** and the ferromagnetic channel region.

When a bias V_{GS} (>0) is applied to the gate electrode, the electric field in the vicinity of the ferromagnetic tunnel barrier **423**b of the source is intensified by the electric flux flowing from the gate electrode to the ferromagnetic source **423**, and the barrier width of the tunnel barrier **423**b in relation to the up-spin electrodes decreases as indicated by d' in FIG. **16**B. Accordingly, the potential barrier transmits the up-spin electrons in ferromagnetic electrode **423**a of the ferromagnetic source, and the up-spin electrons are injected into the channel region located immediately below the gate insulating film. Meanwhile, the down-spin electrons in the non-magnetic electrode **423**a cannot be tunnel-injected, since the barrier height ϕ_s is higher by the spin-split width Δ. Thus, only the up-spin electrons can be injected from the ferromagnetic source **423** by virtue of the ferromagnetic tunnel barrier **423**b.

While being drawn toward the interface between the insulator and the semiconductor by virtue of the bias V_{GS}, the injected electrons are transported to the non-magnetic drain **425** by virtue of the bias V_{DS}, and then form a drain current. Here, the trans (mutual) conductance and the drain current of the MISFET **421** in accordance with this embodiment depends on the relative magnetization direction between the ferromagnetic tunnel barrier **423**b of the ferromagnetic source **423** and the ferromagnetic channel region **427**.

The electrons tunneling from the non-magnetic electrode **423**a of the ferromagnetic source **423** to the ferromagnetic channel region **427** via the ferromagnetic tunnel barrier **423**b have the same effect as a tunneling magneto-resistance (TMR) effect (hereinafter referred to simply as the TMR effect). Accordingly, the tunnel resistance is low in a case where the ferromagnetic source **423** and the ferromagnetic channel region **427** exhibit parallel magnetization, and the tunnel resistance is high in a case of antiparallel magnetization. Even if the influence of the TMR effect is small, electrons with a spin polarization rate that depends on the spin polarization rate of the ferromagnetic source **423** can be injected from the ferromagnetic source **423**. Accordingly, the electrons cause spin-dependent scattering in the ferromagnetic channel region **427**, in accordance with the relative magnetization configuration between the ferromagnetic channel region **427** and the ferromagnetic source **223**. Due to the TMR effect and the spin-dependent scattering in the ferromagnetic channel region **427** at the time of tunnel injection, the trans conductance varies in accordance with the relative magnetization direction between the ferromagnetic source **423** and the ferromagnetic channel region **427**.

As shown in FIG. **16**B, if the ferromagnetic source **423** and the ferromagnetic channel region **427** exhibit parallel magnetization, the trans conductance and the drain current become higher. As shown in FIG. **16**C, if the ferromagnetic source **423** and the ferromagnetic channel region **427** exhibit antiparallel magnetization, the trans conductance and the drain current become low.

As described above, in the MISFET in accordance with this embodiment, the trans conductance can be controlled by the relative magnetization direction between the ferromagnetic source and the ferromagnetic channel region, even with the same bias being applied. Also, the number of carriers to be injected into the channel region can be controlled by the bias V_{GS}, and accordingly, the drain current can be controlled by the bias V_{GS}. In this manner, the MISFET in accordance with this embodiment has the characteristics of a regular transistor that can control the drain current with the gate voltage, and can also control the trans conductance in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic channel region.

Next, a memory cell employing a MISFET in accordance with a fourteenth embodiment of the present invention is described, with reference to the accompanying drawings. FIG. **17** illustrates a memory cell structure in accordance with this embodiment. This memory cell structure is a compound structure formed with a gate electrode and a word line, utilizing a yoke structure. FIG. **17** is a cross-sectional view of the

MISFET of any of the seventh through thirteenth embodiments of the present invention, seen from the source side or the drain side. As shown in FIG. **17**, the memory cell structure **431** in accordance with this embodiment includes a stacked structure and a yoke **445** that externally covers the stacked structure. The stacked structure is formed with a channel region **433**, a gate oxide film **435** formed on the channel region **433**, a gate electrode **437** formed on the gate oxide film **435**, and a word line **441** formed on the gate electrode **437**. The yoke **445** is preferably made of a high magnetic permeability material. Using the structure shown in FIG. **17**, the magnetic field generated by the current of the word line **441** can be effectively applied to the ferromagnetic channel region **433**, and accordingly, the write current required in the memory can be reduced.

Next, a non-volatile memory employing the MISFET of any of the foregoing embodiments is described. Each of the above described MISFETs stores binary information by switching the relative magnetization configuration of the ferromagnetic source (or the ferromagnetic drain) and the ferromagnetic channel region (ferromagnetic semiconductor layer) between parallel magnetization and antiparallel magnetization, and can detect the magnetization configuration, based on the output (the drain current) representing the relative magnetization configuration. Thus, each of the above described MISFETs can be employed in a non-volatile memory. Since a 1-bit memory cell can be formed with a single MISFET, high integration can be realized. Also, the write current, which has been a serious problem in conventional MRAMs, can be reduced by actively utilizing the magnetism control by virtue of the field effect of the ferromagnetic semiconductor used for the channel region (see Non-Patent Documents 2 and 3).

In the following, the operation principles of the above described non-volatile memory that employs an n-channel MISFET having a ferromagnetic source are described. However, the same memory operation can be performed with a MISFET of the other structures or a p-channel device. In the following description, the ferromagnetic source is a pin layer having a fixed magnetization direction, and the ferromagnetic channel region is a free layer having a varying magnetization direction.

FIG. **18**A illustrates an example structure of a non-volatile memory in accordance with a fifteenth embodiment of the present invention. As shown in FIG. **18**A, a memory cell group **471** in accordance with this embodiment includes memory cells that are MISFETs **473** of one of the foregoing embodiments, word lines WL that are connected to the gate electrodes G of the MISFETs **473**, bit lines BL that are connected to the drains D of the MISFETs **473**, and ground lines GND that are connected to the sources of the MISFETs **473**. In a rewrite operation in a selected one of the memory cells, a relatively high bias voltage ("high" in relation to the substrate potential or the gate electrode) is applied to the bit line BL and the ground line GND to which the selected cell is connected. By doing so, the number of carriers is reduced to such an extent that the ferromagnetism of the channel region vanishes and paramagnetism appears (with the coercive force becoming sufficiently small), or depletion is caused. The bit line BL and the ground line GND are arranged to cross each other at right angles as shown in FIG. **18**A, so as to apply bias to the source S and the drain D only in the selected cell. In the unselected cell also connected to the bit line BL or the ground line GND, the bias is applied only to either the drain D or the source S. Therefore, the bias should be set so that the ferromagnetism cannot entirely vanish in the channel only with the bias application to either the drain or the source (for example, the region extending from the source S to the center, or the region extending from the drain D to the center, should be depleted). In this manner, the magnetization information in the unselected cells can be maintained (for example, the volume of the channel region is adjusted to such a size that a single magnetic domain structure can be easily realized).

In this situation, a relatively low current is applied to the word line WL, so as to induce a magnetic field and change the magnetization direction of the channel region in the paramagnetic state. The bias between the bit line BL and the ground line GND is then cut off, so that the channel region returns to the ferromagnetic state. Thus, the information is rewritten.

FIG. **19** illustrates the principles of the above rewrite operation, showing a magnetization curve. First, it is assumed that the magnetization of the channel region formed with a ferromagnetic semiconductor layer is represented by the point A on the magnetization curve. In this state, rewrite to the point E in FIG. **19** is to be performed. When the magnetization is represented by the point A, bias are applied to the bit line BL and the ground line GND, so that the ferromagnetism of the selected cell is changed to paramagnetism. At this point, the magnetization of the channel region is represented by the point B. A current is then applied to the word line WL connected to the gate electrode G located immediately above the channel region. With this current, the magnetization inversion to the point C in FIG. **19** can be realized, even if the intensity of the magnetic field induced by the current is smaller than the coercive force H_C of the channel region in the ferromagnetic state. While the current flows in the gate electrode G, the bias applied to the source S and the drain D is cut off to return the channel region to the ferromagnetic state. At this point, the magnetization direction of the paramagnetic state is maintained as indicated by the point D in FIG. **19**. The current applied to the word line WL is cut off in this situation, thereby completing the rewrite operation (represented by the point E in FIG. **19**).

In the memory cell in accordance with this embodiment, magnetization inversion can be performed with a magnetic field of a lower intensity than the coercive force of the channel region in a ferromagnetic state. Accordingly, the current required for magnetization inversion can be greatly reduced. Also, as rewrite is performed only in the selected cell that has been put into a paramagnetic state, false rewrite cannot be often caused.

An information rewrite operation can also be performed with low current, utilizing initial magnetization characteristics. In a ferromagnetic semiconductor, the number of carriers is reduced by a field effect to eliminate the ferromagnetism. By doing so, the ferromagnetic semiconductor can be demagnetized. As a magnetic field is induced in this situation, the magnetization curve exhibits an initial magnetization curve that is to be utilized. FIG. **20** illustrates such a rewrite operation, showing a magnetization curve. At first, the magnetization of the channel region is represented by the point A' on the magnetization curve. In this situation, rewrite to the point E' in FIG. **20** is to be performed. First, biases are applied to the bit line BL and the ground line GND, so as to reduce the number of carriers in the ferromagnetic semiconductor layer. By doing so, the ferromagnetic channel of the selected cell is demagnetized. At this point, the magnetization of the channel region is represented by the point B'. After the bias applied to the bit line BL and the ground line GND is cut off, a current is applied to the word line WL connected to the gate electrode G located immediately above the channel region, so that the magnetization along the initial magnetization curve passing through the point C' in FIG. **20** can be performed even if the intensity of the magnetic field induced by the current is

smaller than the coercive force HC of the channel region in the ferromagnetic state. Thus, magnetization inversion can be performed with a magnetic field with lower intensity than HC (represented by the point D' in FIG. **20**). The current to the gate electrode G is then cut off, thereby completing the rewrite operation (represented by the point E' in FIG. **20**).

In an information readout operation, a bias required for a regular operation of a transistor is applied to the selected cell, and the relative magnetization configuration between the ferromagnetic source and the ferromagnetic channel region is detected based on the intensity of the drain current. Since the word line WL and the bit line BL cross each other at right angles, stored contents can be read out only from the selected cell. In the readout operation, the required bias may be applied through precharging.

Next, a memory cell that employs MISFETs in accordance with a sixteenth embodiment of the present invention is described, with reference to the accompanying drawings. FIG. **18**B illustrates a memory cell structure in accordance with this embodiment, using MISFETS of any of the foregoing embodiments. A memory cell group **481** in accordance with this embodiment includes memory cells **483** each having a pair of MISFETs **483***a* and **483***b* adjacent to each other in the column direction, word lines WL that are connected to the gate electrodes G of the MISFETs **483***a* and **483***b*, a first bit line BL**1** connected to the drain D of each MISFET **483***a*, a second bit line BL**2** connected to the drain D of each MISFET **483***b*, and ground lines GND connected to the sources S. The MISFETs **483***a* and **483***b* are MISFETs in accordance with any of the seventh through fourteenth embodiments. With the memory cell structure using MISFETs in accordance with this embodiment, a source is shared between each two adjacent MISFETs. Accordingly, the area of each cell can be effectively reduced.

Next, a non-volatile memory in accordance with a seventeenth embodiment of the present invention is described, with reference to the accompanying drawings. FIG. **21**A illustrates the non-volatile memory in accordance with this embodiment, which is an example cell structure that can collectively erase and rewrite two or more memory cells. The non-volatile memory in accordance with this embodiment includes MISFETs in accordance with any of the seventh through fourteenth embodiments of the present invention, word lines WL, bit lines BL, and ground lines GND. In this structure, the bit lines BL connected to the drains are arranged in parallel with the ground lines GND connected to the sources. In the cell structure shown in FIG. **21**A, all the magnetization information stored in the MISFETs that are aligned in parallel with each other and are connected to a selected one of the bit lines can be erased and rewritten at once.

In a rewrite operation, biases are applied to the selected bit line BL and the ground line GND connected to the MISFETs connected to the selected bit line BL, and the channel regions of all the MISFETs connected to the selected bit line BL and the ground line GND are changed from a ferromagnetic state to a paramagnetic state (or a state with sufficiently small coercive force). A current in accordance with the contents of the rewrite is then applied to the word lines WL connected to the gates of the MISFETs, so that the magnetization direction of the channel region in the paramagnetic state is changed. The application of the bias to the bit line BL and the ground line GND is then cut off, thereby returning the channel region of each of the MISFETs to a ferromagnetic state. Lastly, the application of current to each word line, and the information rewrite is completed. In the memory cell structure in accordance with this embodiment, the current required for rewriting each memory cell is low, and accordingly, rewrite current can be applied simultaneously to a large number of word lines WL. Thus, the magnetization information stored in a large number of MISFETs connected to one bit line BL can be rewritten at once. In this manner, a rewrite operation can be performed at a higher speed. Since the word lines WL are perpendicular to the bit lines BL in the above described cell structure, the magnetization configuration of a selected cell can be detected based on a drain current representing the magnetization configuration, upon application of a regular bias to the selected cell. In this cell structure, it is also possible to perform a readout operation through precharging.

Also, a low-current write operation is possible with the above memory cell structure, using the initial magnetization characteristics described in conjunction with FIG. **20**. In such a case, the contents of the memory cells connected to a selected bit line BL are collectively erased, and write can be performed one bit at a time. Accordingly, a rewrite method that is similar to the method employed in a flash memory can be used. More specifically, biases are applied to a selected bit line BL and the corresponding ground line GND, so that the ferromagnetic channel regions of the memory cells connected to the selected bit line BL are collectively demagnetized. After the application of biases to the bit line BL and the ground line GND is cut off, a current is sequentially applied to the word lines WL connected to the gate electrodes G of the demagnetized memory cells, thereby performing rewrite bit by bit. This rewrite method is advantageous in that the current required for each one memory cell is low, because rewrite is performed one bit at a time.

Next, a non-volatile memory in accordance with an eighteenth embodiment of the present invention is described, with reference to the accompanying drawings. The structure shown in FIG. **21**B has the same structure as the memory cell structure shown in FIG. **21**A, except in that each source S is shared by two adjacent MISFETs **463***a* and **463***b* aligned in the column direction, and each shared source S is connected to a ground line GND. The drains D of the two MISFETs **463***a* and **463***b* sharing one source S are connected to different bit lines BL**1** and BL**2**. The structure illustrated in FIG. **21**B is advantageous in that the area of each cell can be made smaller, and the area of the integrated circuit can also be reduced.

Although the embodiments of the present invention have been described, the present invention is not limited to those specific examples. It should be obvious to those skilled in the art that various changes and modification can be made to those embodiments.

A MISFET having a ferromagnetic semiconductor as a channel region in accordance with the present invention characteristically serves as a transistor that can control a drain current through a gate voltage, and can also control the trans conductance through the relative magnetization direction between the ferromagnetic channel region and the ferromagnetic source (or the ferromagnetic drain, or both the ferromagnetic source and the ferromagnetic drain). Accordingly, binary information can be stored in accordance with the relative magnetization direction, and the relative magnetization direction can be electrically detected. Also, using the magnetization control by virtue of the field effect of the channel region formed with a ferromagnetic semiconductor, the amount of current required for information rewrite can be greatly reduced. Accordingly, any of the above described MISFETs can form a high-performance non-volatile memory cell that is suitable for high integration.

Although the embodiments of the present invention have been described so far, the present invention is not limited to them. It should be obvious to those skilled in the art that various changes and modifications can be made to them.

INDUSTRIAL APPLICABILITY

The present invention can be applied to the non-volatile memory devices for various electronic devices, especially for portable electronic devices, which are suitable for higher integration and lower power consumption.

The invention claimed is:

1. A transistor comprising:

a source (a "ferromagnetic source") that is made of a ferromagnetic material and injects carriers;

a drain that receives the carriers injected from the ferromagnetic source;

a tunnel barrier (a "ferromagnetic tunnel barrier") that is located between the ferromagnetic source and the drain and is made of a ferromagnetic material; and

a gate electrode that is formed in relation to the ferromagnetic tunnel barrier, and controls carrier conduction from the ferromagnetic source to the drain by inducing an electric field in the ferromagnetic tunnel barrier,

the energy band edge of the conduction band in the ferromagnetic tunnel barrier being spin-split when the carriers are electrons,

the energy band edge of the valence band in the ferromagnetic tunnel barrier being spin-split when the carriers are holes.

2. The transistor as claimed in claim **1**, further comprising:

a gate insulating film that is formed between the ferromagnetic tunnel barrier and the gate electrode.

3. The transistor as claimed in claim **1**, wherein:

the ferromagnetic tunnel barrier exhibits a low tunnel barrier to the major-spin electrons in the ferromagnetic source when the magnetization direction of the ferromagnetic tunnel barrier is the same as the magnetization direction of the ferromagnetic source or the direction of the major spin in the ferromagnetic source is the same as the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier (the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier being "parallel magnetization"); and

the ferromagnetic tunnel barrier exhibits a high tunnel barrier to the major-spin electrons in the ferromagnetic source when the magnetization direction of the ferromagnetic tunnel barrier is opposite to the magnetization direction of the ferromagnetic source or the direction of the major spin in the ferromagnetic source is different from the spin direction of the spin band at the energy band edge of the ferromagnetic tunnel barrier (the relative magnetization direction being "parallel magnetization").

4. The transistor as claimed in claim **1**, wherein the ferromagnetic tunnel barrier has a tunnel probability that can be controlled in relation to the major spin in the ferromagnetic source, in accordance with a voltage to be applied to the gate electrode (the voltage being "gate voltage"), when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization.

5. The transistor as claimed in claim **1**, wherein the ferromagnetic tunnel barrier has such a thickness that the major spin in the ferromagnetic source tunneling the ferromagnetic tunnel barrier generates a current through application of a gate voltage to the ferromagnetic tunnel barrier, when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization.

6. The transistor as claimed in claim **1**, wherein a threshold voltage is set as such a gate voltage as to generate a predetermined current between the ferromagnetic source and the drain through application of a gate voltage, when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the parallel magnetization.

7. The transistor as claimed in claim **1**, wherein, when the ferromagnetic source and the ferromagnetic tunnel barrier exhibit the antiparallel magnetization, a current generated between the ferromagnetic source and the ferromagnetic drain is lower than a current caused in the case of the parallel magnetization, the current in the case of the antiparallel magnetization being caused because the barrier height of the ferromagnetic tunnel barrier in relation to the major-spin electrons in the ferromagnetic source is higher by the width of a spin split caused at the energy band edge.

8. The transistor as claimed in claim **1**, wherein mutual conductance can be controlled in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier, with the same bias being applied.

9. The transistor as claimed in claim **1**, wherein the source is made of a half-metal ferromagnetic material, or the source and the drain are made of a half-metal ferromagnetic material.

10. The transistor as claimed in claim **1**, further comprising a non-magnetic member between the ferromagnetic source and the ferromagnetic tunnel barrier.

11. The transistor as claimed in claim **1**, wherein the drain is either a non-magnetic member or a ferromagnetic member.

12. A memory element comprising:

a transistor as claimed in claim **1**,

the memory element storing information in accordance with the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier,

the memory element detecting information stored in the transistor in accordance with output characteristics based on the mutual conductance of the transistor, the mutual conductance depending on the relative magnetization direction between the ferromagnetic source and the ferromagnetic tunnel barrier.

13. A memory element comprising:

a transistor as claimed in claim **1**;

a first line that grounds the ferromagnetic source;

a second line that is connected to the drain; and

a third line that is connected to the gate electrode.

14. A memory element comprising:

a transistor as claimed in claim **1**;

a first line that grounds the ferromagnetic source;

a second line that is connected to the drain;

a third line that is connected to the gate electrode; and

a fourth line that is connected to an output terminal that is formed at one end of the second line, and to a power source via a load, the fourth line branching out from the second line.

15. The memory element as claimed in claim **13**, further comprising:

a first extra line and a second extra line that cross each other on the transistor, while being electrically insulated from each other.

16. The memory element as claimed in claim **15**, wherein the first extra line and the second extra line are replaced with the second line and the third line, or one of the first extra line and the second extra line is replaced with one of the second line and the third line.

17. The memory element as claimed in claim **15**, wherein the memory element rewrites information by converting the magnetization of the ferromagnetic source or the ferromagnetic tunnel barrier to change the relative magnetization configuration of the ferromagnetic tunnel barrier with respect to

the ferromagnetic source, using a magnetic field that is induced by flowing currents to the first extra line and the second extra line, or to the second line and the third line replacing the first extra line and the second extra line, or to one of the second line and the third line replacing one of the first extra line and the second extra line, and one of the first extra line and the second extra line that is not replaced.

18. The memory element as claimed in claim **15**, wherein the memory element reads out information, based on the output characteristics of the transistor, the output characteristics being obtained by applying a first bias to the third line and applying a second bias between the first line and the second line.

19. The memory element as claimed in claim **14**, wherein the memory device read out information in accordance with an output voltage that is obtained based on a voltage decrease in the load due to a current via the load and the transistor, the current being generated between the power source and the first line, when the first bias is applied to the third line.

20. A memory circuit comprising:

transistors as claimed in claim **1**, the transistors being arranged in a matrix fashion;

first lines that ground the ferromagnetic sources of the transistors independently of one another;

a plurality of word lines that are collectively connected to the gate electrodes of the transistors that are aligned in a column direction; and

a plurality of bit lines that are collectively connected to the ferromagnetic drains of the transistors that are arranged in a row direction.

21. A memory circuit comprising:

transistors as claimed in claim **1**, the transistors being arranged in a matrix fashion;

first lines that grounds the ferromagnetic sources of the transistors independently of one another;

a plurality of word lines that are collectively connected to the gate electrodes of the transistors that are aligned in a column direction;

a plurality of bit lines that are collectively connected to the drains of the transistors that are aligned in a row direction;

output terminals each formed at one end of each corresponding one of the bit lines; and

second lines that branch out from the bit lines and are connected to a power source via a load.

22. The memory circuit as claimed in claim **20**, further comprising:

first extra lines and second extra lines that cross each other on the transistors, while being insulated from each other.

23. The memory circuit as claimed in claim **22**, wherein the first extra lines and the second extra lines are replaced with the word lines and the bit lines, or either the first extra lines or the second extra lines are replaced with either the word lines or the bit lines.

24. The memory circuit as claimed in claim **22**, wherein information is rewritten by converting the magnetization of the ferromagnetic source or the ferromagnetic tunnel barrier to change the relative magnetization configuration of the ferromagnetic tunnel barrier with respect to the ferromagnetic source, using a magnetic field that is induced by flowing currents to the first extra line and the second extra line, or to the second line and the third line replacing the first extra line and the second extra line, or to one of the second line and the third line replacing one of the first extra line and the second extra line, and one of the first extra line and the second extra line that is not replaced.

25. The memory circuit as claimed in claim **20**, wherein information is read out based on the output characteristics of the transistor, the output characteristics being obtained by applying a first bias to the word line and applying a second bias between the first line and the bit line.

26. The memory circuit as claimed in claim **21**, wherein information is read out in accordance with an output voltage that is obtained based on a voltage decrease in the load due to a current via the load and the transistor, the current being generated between the power source and the first line, when the first bias is applied to the word line.

27. A memory device comprising:

a first transistor and a second transistor as claimed in claim **1**;

a first line that grounds a ferromagnetic source shared between the first and second transistors;

a second line and a third line that are connect to the drain of the first transistor and the drain of the second transistor; and

a fourth line that is connected to the gate electrode of the first transistor and the gate electrode of the second transistor.

28. A memory circuit comprising:

transistors as claimed in claim **1**, the transistors being arranged in a matrix fashion, the ferromagnetic sources of the transistors being collectively connected to the substrates or contact layers formed on the sides of the substrates and being grounded;

bit lines that are collectively connected to the drains of the transistors that are aligned in a row direction; and

word lines that are collectively connected to the gate electrodes of the transistors that are aligned in a column direction.

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