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(54) **MEMORY CIRCUIT PROVIDED WITH BISTABLE CIRCUIT AND NON-VOLATILE ELEMENT**

SPEICHERSCHALTUNG MIT BISTABILER SCHALTUNG UND NICHTFLÜCHTIGEM ELEMENT

CIRCUIT MÉMOIRE POURVU D'UN CIRCUIT BISTABLE ET D'UN ÉLÉMENT NON VOLATILE

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- **YUSUKE SHUTO ET AL: "Evaluation and Control of Break-Even Time of Nonvolatile Static Random Access Memory Based on Spin-Transistor Architecture with Spin-Transfer-Torque Magnetic Tunnel Junctions", JAPANESE JOURNAL OF APPLIED PHYSICS, vol. 51, 30 March 2012 (2012-03-30), page 040212, XP055167553, ISSN: 0021-4922, DOI: 10.1143/JJAP.51.040212**

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Description

TECHNICAL FIELD

[0001] The present invention relates to memory circuit, and more particularly, to a memory circuit that provided with bistable circuit and nonvolatile element, for example.

BACKGROUND ART

[0002] In a known memory device, data written in a bistable circuit of a SRAM (Static Ramdom Access Memory) is stored into a ferromagnetic tunnel junction element (MTJ) in a nonvolatile manner, to cut off the power supply to the bistable circuit. After that, when the bistable circuit is turned on, the data is restored into the bistable circuit from the MTJ (see Patent Document 1, for example). Power consumption can be reduced by using this memory device in a microprocessor, a system-on-chip, a microcontroller, an FPGA (Field Programmable Gate Array), a CMOS (Complementary Metal Oxide Semiconductor) logic, or the like.

PRIOR ART DOCUMENT

[0003] Document of YUSUKE SHUTO ET AL, "Evaluation and Control of Break-Even Time of Nonvolatile Static Random Access Memory Based on Spin-Transistor Architecture with Spin-Transfer-Torque Magnetic Tunnel Junctions" (JAPANESE JOURNAL OF APPLIED PHYSICS, vol. 51, 30 March 2012 (2012-03-30), page 040212), discloses energy performance of a nonvolatile static random access memory (NV-SRAM) cell for power gating applications analyzed using the performance index of break-even time (BET). The NV-SRAM cell is based on spin-transistor architecture using ordinary metal-oxide-semiconductor field-effect transistors (MOSFETs) and spin-transfer-torque magnetic tunnel junctions (STT-MTJs), whose circuit representation of spin-transistor is referred to as a pseudo-spin-MOSFET (PS-MOSFET).

PATENT DOCUMENT

[0004] Patent Document 1: International Publication Pamphlet WO 2009/028298 A

SUMMARY OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0005] In the memory circuit disclosed in Patent Document 1, data in a bistable circuit can be stored into an MTJ in a nonvolatile manner, and accordingly, the power supply to the bistable circuit can be cut off. As a result, standby power consumption can be dramatically reduced. While power is being supplied, however, power consumption is larger than that with a conventional SRAM.

[0006] The present invention has been made in view of the above problem, and aims to reduce power consumption.

MEANS FOR SOLVING THE PROBLEM

[0007] The present invention is a memory circuit that includes: a bistable circuit that writes stores data; a nonvolatile element that stores data witten in the bistable circuit in a nonvolatile manner and restores data written in a nonvolatile manner into the bistable circuit by changing a resistance value with a current flowing between one end and the other end, the nonvolatile element having the one end connected to a node in the bistable circuit and the other end connected to a control line; an FET that has the source and the drain connected in series to the nonvolatile element between the node and the control line; and a control unit that makes a highest voltage to be applied to the gate of the FET during a period to restore data stored in the nonvolatile element in a nonvolatile manner into the bistable circuit lower than a voltage of a node being at a high level in the bistable circuit during a period to write data into and read data from the bistable circuit in a volatile manner. According to the present invention, power consumption can be reduced.

[0008] In the above structure, the control unit may make the highest voltage to be applied to the gate during a period to store data written in the bistable circuit into the nonvolatile element in a nonvolatile manner lower than the voltage of a node being at a high level in the bistable circuit during the period to write data into and read data from the bistable circuit in a volatile manner.

[0009] In the above structure, the control unit may make the highest voltage to be applied to the control line during a period to store data written in the bistable circuit into the nonvolatile element in a nonvolatile manner lower than the voltage of a node being at a high level in the bistable circuit during the period to write data into and read data from the

bistable circuit in a volatile manner.

EFFECTS OF THE INVENTION

[0010] According to the present invention, power consumption can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]

FIGs. 1A and 1C are diagrams showing an example of a ferromagnetic tunnel junction element, and FIG. 1B is a diagram showing the current-voltage characteristics of the ferromagnetic tunnel junction element 40;
FIG. 2 is a circuit diagram of a memory cell;
FIG. 3 is a timing chart showing control of the memory cell;
FIGs. 4A and 4B are circuit diagrams showing other examples of memory cells;
FIGs. 5A and 5B are block diagrams showing a memory circuit and a memory cell according to a first embodiment;
FIG. 6 is a timing chart showing the voltages of a power supply and a control line;
FIG. 7 is a diagram showing the results of simulations performed to simulate leakage currents from memory cells relative to a power supply;
FIG. 8 is a schematic diagram showing a comparison between a shut-down state and a sleep state in terms of current consumption in the memory circuit according to the first embodiment;
FIG. 9 is a schematic diagram showing a comparison between the memory circuit according to the first embodiment and a 6T-SRAM in terms of current consumption;
FIG. 10 is a flowchart showing control by the control unit;
FIG. 11 is a timing chart showing simulations performed to simulate the voltages of a control line CTRL and a switch line SR during a store period, and currents I1 and 12 flowing in ferromagnetic tunnel junction elements MTJ1 and MTJ2 during the store period;
FIGs. 12A and 12B are diagrams each showing simulations performed to simulate characteristics of a bistable circuit during the store period;
FIG. 13 is a timing chart showing simulations performed to simulate the voltages of a power supply Vsupply and the switch line SR during a restore period, and currents I1 and I2 flowing in the ferromagnetic tunnel junction elements MTJ1 and MTJ2 during the restore period; and
FIGs. 14A through 14C are diagrams each showing simulations performed to simulate changes in potential at nodes Q and QB during the restore period.

MODES FOR CARRYING OUT THE EMBODIMENTS

[0012] First, a ferromagnetic tunnel junction element is described as a nonvolatile element. FIG. 1A is a diagram showing an example of a ferromagnetic tunnel junction element. The ferromagnetic tunnel junction element 40 includes a ferromagnetic electrode free layer 42, a ferromagnetic electrode pinned layer 46, and a tunnel insulator 44 interposed between the ferromagnetic electrode free layer 42 and the ferromagnetic electrode pinned layer 46. The ferromagnetic electrode free layer 42 and the ferromagnetic electrode pinned layer 46 are made of a ferromagnetic metal, a half-metallic ferromagnet, or a ferromagnetic semiconductor. The ferromagnetic electrode free layer 42 has a variable magnetization direction. On the other hand, the ferromagnetic electrode pinned layer 46 has a pinned magnetization direction. A state where the magnetization directions of the ferromagnetic electrode free layer 42 and the ferromagnetic electrode pinned layer 46 are parallel to each other is referred to as a parallel magnetization, and a state where the magnetization directions are antiparallel to each other is referred to as an antiparallel magnetization.

[0013] FIG. 1B is a diagram showing the current-voltage characteristics of the ferromagnetic tunnel junction element 40. As shown in FIG. 1A, a voltage that is applied to the ferromagnetic electrode free layer 42 with respect to the ferromagnetic electrode pinned layer 46 is defined as a voltage V, and a current flowing from the ferromagnetic electrode free layer 42 to the ferromagnetic electrode pinned layer 46 is defined as a current I. Symbols in the ferromagnetic tunnel junction element 40 at this point are defined as shown in FIG. 1C. As shown in FIG. 1B, the resistance Rp of the ferromagnetic tunnel junction element 40 in a parallel magnetization state is lower than the resistance Rap of the ferromagnetic tunnel junction element 40 in an antiparallel magnetization state. In general, Rp and Rap are functions of voltages applied to ferromagnetic tunnel junctions, but will be hereinafter regarded as resistances that have approximately constant resistance values. The following discussion applies even to cases where Rp and Rap are not constant resistances.

[0014] In an antiparallel magnetization state, when the voltage V to be applied to the ferromagnetic tunnel junction

element 40 becomes higher, the current I increases at the rate equivalent to the reciprocal of the resistance Rap (A in FIG. 1B). When the current I exceeds a threshold current I_{TF}, the magnetization of the ferromagnetic electrode free layer 42 is reversed due to the majority-spin electrons of the ferromagnetic electrode pinned layer 46 injected from the ferromagnetic electrode pinned layer 46 into the ferromagnetic electrode free layer 42, and a parallel magnetization state appears (B in FIG. 1B). As a result, the resistance of the ferromagnetic tunnel junction element 40 becomes Rp. In a parallel magnetization state, when the current I flows (C in FIG. 1B) and exceeds the threshold current I_{TR} in the negative direction, the minority-spin electrons of the ferromagnetic electrode free layer 42 among the electrons to be injected from the ferromagnetic electrode free layer 42 into the ferromagnetic electrode pinned layer 46 are reflected by the ferromagnetic electrode pinned layer 46. As a result, the magnetization of the ferromagnetic electrode free layer 42 is reversed, and an antiparallel magnetization state appears (D in FIG. 1B).

[0015] The method of reversing the magnetization direction of the ferromagnetic electrode free layer 42 by changing the magnetization direction through spin-polarized charge injection is called a spin-injection magnetization switching method. The spin-injection magnetization switching method has a higher possibility of reducing the power consumption required to change a magnetization direction than a method of changing a magnetization direction by generating a magnetic field. Also, unlike the method of changing a magnetization direction by generating a magnetic field, the spin-injection magnetization switching method does not have the problem of leakage magnetic fields. Accordingly, the spin-injection magnetization switching method is hardly affected by disturbances that cause inadvertent writing or erasing in cells other than selected cells, and is suitable for large-scale integration.

[0016] Next, an example of a memory cell that includes a bistable circuit and ferromagnetic tunnel junction elements is described. FIG. 2 is a circuit diagram of the memory cell. As shown in FIG. 2, the memory cell 100 includes a first inverter circuit 10, a second inverter circuit 20, and ferromagnetic tunnel junction elements MTJ1 and MTJ2. The first inverter circuit 10 and the second inverter circuit 20 are connected in a ring-like manner, to form a bistable circuit 30. The first inverter circuit 10 includes an n-MOSFET (Metal Oxide Semiconductor Field Effect Transistor) m2 and a p-MOSFET m1. The second inverter circuit 20 includes an n-MOSFET m4 and a p-MOSFET m3.

[0017] The nodes to which the first inverter circuit 10 and the second inverter circuit 20 are connected are nodes Q and QB. The node Q and the node QB are complementary to each other, and the bistable circuit 30 is put into a stable state when the node Q and the node QB are at a high level and a low level, respectively, or when the node Q and the node QB are at a low level and a high level, respectively. The bistable circuit 30 is capable of storing data when in a stable state.

[0018] The nodes Q and QB are connected to input/output lines D and DB via MOSFETs m5 and m6, respectively. The gates of the MOSFETs m5 and m6 are connected to a word line WL. The MOSFETs m1 through m6 form a 6-MOSFET SRAM.

[0019] An FET m7 and the ferromagnetic tunnel junction element MTJ1 are connected between the node Q and a control line CTRL, and an FET m8 and the ferromagnetic tunnel junction element MTJ2 are connected between the node QB and the control line CTRL. One of the source and the drain of each of the FETs m7 and m8 is connected to the node Q/QB, and the other one of the source and the drain is connected to the ferromagnetic tunnel junction element MTJ1/MTJ2. The gates of the FETs m7 and m8 are connected to a switch line SR. Each of the FETs m7 and m8 may be connected between the ferromagnetic tunnel junction element MTJ1/MTJ2 and the control line CTRL. That is, the source and the drain of each of the FETs m7 and m8 should be connected in series to the ferromagnetic tunnel junction element MTJ1/MTJ2 between the nodes Q/QB and the control line CTRL. Alternatively, the FETs m7 and m8 may not be provided.

[0020] Data is written into and read from the bistable circuit 30 in the same manner as with a conventional SRAM. Specifically, the word line WL is set at a high level to put the FETs m5 and m6 into a conduction state, and data in the input/output lines D and DB is written into the bistable circuit 30. The input/output lines D and DB are put into an equipotential floating state, and the word line WL is set at a high level to put the FETs m5 and m6 into a conduction state. In this manner, data in the bistable circuit 30 can be read into the input/output lines D and DB. Data is held in the bistable circuit 30 by putting the FETs m5 and m6 into a cut-off state. When data writing, reading, or holding is performed in the bistable circuit 30, it is preferable to set the switch line SR at a low level, and put the FETs m7 and m8 into a cut-off state. As a result, the current flowing between the nodes Q and QB and the control line CTRL can be reduced, and power consumption can be lowered.

[0021] FIG. 3 is a timing chart illustrating control of the memory cell. The shaded region indicates a region in which it is not clear whether the level is high or low. As shown in FIG. 3, a supply voltage Vsupply is supplied, and the control line CTRL and the switch line SR are at a low level. Data is written into the bistable circuit 30 by setting the word line WL at a high level and setting the input/output lines D and DB at a high or low level. Data is stored from the bistable circuit 30 into the ferromagnetic tunnel junction elements MTJ1 and MTJ2 by setting the switch line SR and the control line CTRL at a high level during a time period T1, and setting the switch line SR and the control line CTRL at a high level and low level, respectively during a time period T2.

[0022] When the nodes Q and QB are at a high level and a low level, respectively, the ferromagnetic tunnel junction

elements MTJ1 and MTJ2 have a high resistance and a low resistance, respectively. When the nodes Q and QB are at a low level and a high level, respectively, the ferromagnetic tunnel junction elements MTJ1 and MTJ2 have a low resistance and a high resistance, respectively. In this manner, data in the bistable circuit 30 is stored into the ferromagnetic tunnel junction elements MTJ1 and MTJ2.

[0023] After that, the supply voltage Vsupply is set at 0 V, to put the memory cell into a shut-down state. As any current does not flow in the memory cell at this point, power consumption can be lowered. Data is restored into the bistable circuit 30 from the ferromagnetic tunnel junction elements MTJ1 and MTJ 2 by raising the supply voltage Vsupply from 0 V while maintaining the control line CTRL at a low level and the switch line SR at a high level during a time period T3.

[0024] When the ferromagnetic tunnel junction elements MTJ1 and MTJ2 have a high resistance and a low resistance, respectively, the nodes Q and QB are at a high level and a low level, respectively. When the ferromagnetic tunnel junction elements MTJ1 and MTJ2 have a low resistance and a high resistance, respectively, the nodes Q and QB are at a low level and a high level, respectively. In this manner, data stored in the ferromagnetic tunnel junction elements MTJ1 and MTJ2 in a nonvolatile manner is restored into the bistable circuit.

[0025] Data is read from the bistable circuit 30 by setting the word line WL at a high level.

[0026] FIGs. 4A and 4B are diagrams showing other examples of memory cells. As shown in FIG. 4A, a resistor R1 can be used in place of the ferromagnetic tunnel junction element MTJ2. As shown in FIG. 4B, the node QB and the control line CTRL are not connected to each other. As shown in FIGs. 4A and 4B, the ferromagnetic tunnel junction element may be connected only between one of the nodes Q and QB and the control line CTRL. The FET m7 may be connected between the ferromagnetic tunnel junction element MTJ1 and the control line CTRL in each case. Alternatively, the FET m7 may not be provided. In each of the embodiments described below, the memory cell 100 shown in FIG. 2 will be described as an example, but either of the memory cells shown in FIGs. 4A and 4B may be used instead. Although ferromagnetic tunnel junction elements will be described as an example of nonvolatile elements, some other nonvolatile elements such as resistive switching memory elements, phase-change memory elements, or ferroelectric memory elements may be used instead.

[First Embodiment]

[0027] FIGs. 5A and 5B are block diagrams showing a memory circuit and a memory cell according to a first embodiment. As shown in FIG. 5A, a memory circuit 103 includes a memory area 77, a column decoder 71, a column driver 72, a row decoder 73, a row driver 74, and a control unit 85. In the memory area 77, memory cells 75 are arranged in a matrix fashion. The column decoder 71 and the row decoder 73 select a column and a row in accordance with an address signal. The column driver 72 applies a voltage or the like to the input/output lines D and DB of a selected column and the control line CTRL. The row driver 74 applies a voltage or the like to the word line WL of a selected row, the switch line SR, and the control line CTRL. The control unit 85 applies a voltage or the like to the input/output lines D and DB, the word line WL, the switch line SR, and the control line CTRL of a memory cell 75, via the column decoder 71, the column driver 72, the row decoder 73, and the row driver 74. When the column driver 72 applies a voltage to a control line, the control line is connected to each corresponding memory cell. As shown in FIG. 5B, the memory cells 75 are the same as the memory cell 100 shown in FIG. 2, for example.

[0028] When the row driver 74 applies a voltage to a control line CTRL, the control line CTRL is connected to the memory cells 75 arranged in one row. When the column driver 72 applies a voltage to a control line CTRL, the control line CTRL is connected to the memory cells 75 arranged in a column, for example.

[0029] FIG. 6 is a timing chart showing the voltages of a power supply and a control line. As shown in FIG. 6, the time period during which data is held in the bistable circuit 30 is formed with a sleep period and a normal period. The normal period is the time period during which data in the bistable circuit 30 is rewritten in a volatile manner. The sleep period is the time period during which data in the bistable circuit 30 is only held, and is not rewritten. During the sleep period, the supply voltage Vsupply to be supplied to the bistable circuit 30 is made lower than that during the normal period so that data can be held. For example, Vsupply during the normal period is set at 1.1 V, and Vsupply during the sleep period is set at 0.9 V. With this arrangement, power consumption can be lowered.

[0030] If the voltage of the control line CTRL during the sleep period and the normal period is 0 V (a low-level voltage), power consumption increases due to leakage current from the MOSFETs m7 and m8. Therefore, the voltage of the control line CTRL is made higher than 0 V. Accordingly, leakage current from the MOSFETs m7 and m8 can be reduced, and power consumption can be lowered.

[0031] During the store period, the voltage of the control line CTRL is set at 0 V, and thereafter, is set at 1.1 V. During the shut-down period, both the supply voltage Vsupply and the control line CTRL are set at 0 V.

[0032] FIG. 7 is a diagram illustrating simulations performed to simulate leakage currents from memory cells with respect to a power supply. The dotted line indicates the leakage current of a 6-transistor SRAM (6T-SRAM) cell that is the same as the one shown in FIG. 5B, except that the MOSFETs m7 and m8, and the ferromagnetic tunnel junction elements MTJ1 and MTJ2 are not provided. The dashed line indicates the leakage current in a case where the voltage

of the control line CTRL is set at 0 V, and the solid line indicates the leakage current in a case where the voltage of the control line CTRL is set at 0.1 V. As shown in FIG. 7, power consumption by a memory cell can be lowered by controlling the voltage of the control line CTRL.

[0033] FIG. 8 is a schematic diagram showing a comparison between a shut-down state and a sleep state in terms of current consumption in the memory circuit according to the first embodiment. FIG. 9 is a schematic diagram showing a comparison between the memory circuit according to the first embodiment and a 6T-SRAM in terms of current consumption. The solid line in FIG. 8 indicates the current consumption in each time period in the memory circuit 103. The dashed line in FIG. 8 indicates the current consumption in a case where the memory cell 75 is not shut down but is put into a sleep state. In Fig. 9, the solid line indicates the current consumption in each time period in the memory circuit 103. The dashed line indicates the current consumption by a memory circuit using 6T-SRAM cells. The dotted line indicates the current consumption in the normal period in a memory circuit using 6T-SRAM cells.

[0034] The length of the sleep period is represented by τ_{sleep}, the current in a 6T-SRAM is represented by I_{LS}^{V} and the current in the first embodiment is represented by I_{LS}^{NV}. The length of the normal period is represented by τ_{act}, the current in the 6T-SRAM is represented by I_{L}^{V}, and the current in the first embodiment is represented by I_{L}^{NV}. The length of the store period is represented by τ_{st}, and the current is represented by I_{MTJ}. The length of the shut-down period is represented by τ_{SD}, and the current is represented by I_{L}^{SD}. The length of the restore period is represented by τ_{ret}, and the current is represented by I_{Rush}. The total length of the sleep period and the normal period is represented by τ_{exe}. The length from the sleep period to the restore period is represented by τ_{cyc}.

[0035] As shown in FIG. 9, in the sleep period and the regular period, leakage current flows in the MOSFETs m7 and m8, and therefore, the power consumption by the memory circuit 103 of the first embodiment is larger than that by the 6T-SRAM. In the store period and the restore period, current flows in the ferromagnetic tunnel junction elements MTJ1 and MTJ2, and therefore, the power consumption in the first embodiment becomes larger. In the shut-down period, a very small amount of leakage current flows in the memory circuit 103 of the first embodiment, but the power consumption becomes sufficiently smaller. Since the 6T-SRAM cannot be shut down, total of the store period, the shut-down period, and the restore period form the sleep period.

[0036] FIG. 10 is a flowchart showing the control by the control unit. FIG. 10 shows the control to be performed in a case where there is a non-access period during which data is not read from or written into the bistable circuit 30. The control unit 85 acquires the non-access period (step S10). The non-access period is acquired from a CPU (Central Processing Unit) or the like that controls the memory circuit 103, for example. The control unit 85 determines whether the non-access period is longer than a predetermined time period T0 (step S12). If the determination result indicates "Yes", the control unit 85 stores data in the bistable circuit 30 into the ferromagnetic tunnel junction elements MTJ1 and MTJ2 (step S14). After that, the control unit 85 performs shutting-down by cutting off the supply voltage Vsupply (step S16). The control unit 85 determines whether to perform restoring (step S18). If the non-access period has passed, or where a signal to access the memory cell 75 is acquired from the CPU or the like, for example, the control unit 85 determines to perform restoring. If the determination result indicates "Yes", the control unit 85 restores the data stored in the ferromagnetic tunnel junction elements MTJ1 and MTJ2 into the bistable circuit 30 (step S20). After that, the operation comes to an end. If the determination result indicates "No", the operation returns to step S18.

[0037] If the determination result of step S12 indicates "No", the control unit 85 lowers the supply voltage Vsupply for the bistable circuit 30, to put the memory cell 75 into a sleep state (step S22). The control unit 85 determines whether to put the bistable circuit 30 back into a normal state (step S18). In a case where the non-access period has passed, or where a signal to access the memory cell 75 is acquired from the CPU or the like, for example, the control unit 85 determines to put the bistable circuit 30 back into a normal state (step S24). If the determination result indicates "Yes", the control unit 85 puts the supply voltage Vsupply for the bistable circuit 30 back into a normal state, to put the memory cell 75 into a normal state (step S26). The operation then comes to an end. If the determination result indicates "No", the operation returns to step S24.

[0038] According to the first embodiment, when the non-access period is longer than the predetermined time period T0, the control unit 85 stores data written in the bistable circuit 30 in a nonvolatile manner, and cuts off the power supply to the bistable circuit 30, as in steps S14 and S16. When the non-access period is shorter than the predetermined time period T0, data written in the bistable circuit 30 is not stored in a nonvolatile manner, but the supply voltage Vsupply for the bistable circuit 30 is made lower than the voltage to be used in reading data from or writing data into the bistable circuit 30, as in step S22. That is, the memory cell 75 is put into a sleep state. As shown in FIG. 8, current consumption increases during the store period and restore period. Therefore, when the non-access period is shorter, total power consumption can be lowered in a sleep state without shutting-down. When the non-access period is longer, on the other hand, the total power consumption can be lowered by shutting-down. Accordingly, power consumption can be lowered in the first embodiment.

[0039] As the predetermined time period T0, a self-compared break-even period (BET^{SC}) can be used. BET^{SC} is a shut-down period such that the power consumption in a case where the memory cell is shut down during the non-access period becomes equal to the power consumption in a case where the memory cell is put into a sleep state during the

non-access period. For example, BET^{SC} is such a time period that the power consumed when the predetermined time period T0 is the sleep period is equal to the sum of the power consumed during the period to store data into and restore data from the ferromagnetic tunnel junction elements MTJ1 and MTJ2 and the power consumed by the leakage current in a case where the memory cell is shut down during the predetermined time period. To reduce power consumption by the memory circuit 103, the length of the predetermined time period T0 is preferably made equal to or longer than the length of BET^{SC}.

[0040] The leakage current during the shut-down period is the current that flows to prevent the supply voltage from becoming 0 V even when the power supply to the bistable circuit 30 is cut off, for example. Other than that, the leakage current includes the current that flows during the shut-down period. For example, the supply voltage Vsupply during the shut-down period is made 0 V by providing a sleep transistor between the supply voltage Vsupply and the power supply, and switching off the sleep transistor. If there is a small amount of leakage current from the sleep transistor, the leakage current also flows in the memory cell. Therefore, there are cases where the leakage current during the shut-down period cannot be made zero.

[0041] If the power consumption due to the leakage current during the shut-down period is ignorable, BET^{SC} can be a time period during which the power consumption in a case where a sleep state lasts during the predetermined time period T0 is equal to the power consumption during the period to store data into and restore data from the ferromagnetic tunnel junction elements MTJ1 and MTJ2.

[0042] In FIG. 8, a region 50 represents a difference between the current in a storing case and the current in a sleep state. A region 52 represents a difference between the current in a restoring case and the current in a sleep state. The energy equivalent to the region 50 (the energy calculated by subtracting the energy in a case where the memory cell 75 is put into a sleep state during the store period from the energy for storing data into the ferromagnetic tunnel junction elements) is represented by E_{store}^{SC}, and the energy equivalent to the region 52 (the energy calculated by subtracting the energy in a case where the memory cell 75 is put into a sleep state during the restore period from the energy for restoring data from the ferromagnetic tunnel junction elements) is represented by $E_{restore}^{SC}$. The current consumption during the sleep period is represented by I_{LS}^{NV}, the current consumption during the shut-down period is represented by I_L^{SD}, and the supply voltage during the sleep period is represented by V_{sleep}. At this point, the period BET^{SC} can be expressed by Mathematical Formula 1.

[Mathematical Formula 1]

$$BET^{SC} = \frac{E_{store}^{SC} + E_{restore}^{SC}}{\left(I_{LS}^{V} - I_{L}^{SD}\right)V_{sleep}}$$

[0043] In FIG. 9, the energy calculated by subtracting the energy during the time period corresponding to the sleep state of the 6T-SRAM from the necessary energy for storing is represented by E_{store}, and the energy calculated by subtracting the energy during the time period corresponding to the sleep state of the 6T-SRAM from the necessary energy for restoring is represented by $E_{restore}$. The duty ratio during the sleep period is represented by $r_{sleep} = (\tau_{sleep}/\tau_{exe})$. When $\eta_L^V = (I_L^{NV} - I_L^V)/(I_{LS}^V - I_L^{SD})$, $\eta_{LS}^V = (I_{LS}^{NV} - I_{LS}^V)/(I_{LS}^V - I_L^{SD})$, the break-even period BET relative to that of the 6T-SRAM can be expressed by Mathematical Formula 2.

[Mathematical Formula 2]

$$BET = \frac{E_{store} + E_{restore}}{\left(I_{LS}^{V} - I_{L}^{SD}\right)V_{sleep}} + \eta_{LS}^{NV} r_{sleep}\tau_{exe} + \eta_{L}^{NV}\frac{V_{DD}}{V_{sleep}}(1 - r_{sleep})\tau_{exe}$$

[0044] As described above, when the memory circuit according to the first embodiment is compared with a 6T-SRAM in terms of power consumption, a greater power saving effect than that of the 6T-SRAM can be achieved with the time period BET or longer.

[0045] In the first embodiment, an example case where the ferromagnetic tunnel junction elements MTJ1 and MTJ2 are connected between the bistable circuit 30 and the control line CTRL has been described. However, some other circuit structure may be used, as long as data can be stored into a nonvolatile element such as a ferromagnetic tunnel junction element in a nonvolatile manner. For example, a ferromagnetic tunnel junction element may be provided between one of the nodes Q and QB in the bistable circuit 30 and the control line CTRL, as shown in FIGs. 4A and 4B.

[0046] In the case of a nonvolatile element that stores data written in the bistable circuit 30 in a nonvolatile manner

by using a current flowing between both ends as in a ferromagnetic tunnel junction element, the current consumption during the store period is large. Therefore, it is preferable to determine whether to shut down the memory cell based on a comparison between the non-access period and the predetermined time period.

[0047] As shown in FIG. 7, the control unit 85 performs control so that the voltage of the control line CTRL during the period for the bistable circuit 30 to store data (the sleep period and the normal period) becomes higher than the lowest voltage to be applied to the control line CTRL during the period to store the data written in the bistable circuit 30 into a nonvolatile element in a nonvolatile manner (the store period). In this manner, power consumption by the memory cell 75 can be lowered.

[0048] Also, as shown in FIG. 7, the control unit 85 performs control so that the voltage of the control line CTRL during the period for the bistable circuit 30 to store data becomes higher than the voltage of the control line CTRL during the period to cut off the power supply to the bistable circuit 30 (the shut-down period). In this manner, power consumption by the memory cell can be lowered.

[Second Embodiment]

[0049] The structure of a memory circuit of a second embodiment is the same as that of the first embodiment illustrated in FIG. 5, and therefore, explanation thereof is not repeated herein. FIG. 11 is a timing chart illustrating simulations performed to simulate the voltages of the control line CTRL and the switch line SR during the store period, and the currents I1 and I2 flowing in the ferromagnetic tunnel junction elements MTJ1 and MTJ2 during the store period. The simulations were performed in cases where the ferromagnetic tunnel junction element MTJ1 was switched from a low resistance to a high resistance, and the ferromagnetic tunnel junction element MTJ2 was switched from a high resistance to a low resistance. The dotted lines indicate a case where the voltages of the control line CTRL and the switch line SR were 1.1 V (VDD), the dashed lines indicate a case where the voltages of the control line CTRL and the switch line SR were 1.1 V and 0.7 V, respectively, and the solid lines indicate a case where the voltages of the control line CTRL and the switch line SR were 0.4 V and 0.7 V, respectively.

[0050] The currents I1 and I2 are positive currents when flowing from the bistable circuit 30 to the control line CTRL. A current Ic is the current with which the resistance of each ferromagnetic tunnel junction element changes. That is, when the absolute values of the currents I1 and I2 are greater than the current Ic, the resistance of each ferromagnetic tunnel junction element changes.

[0051] Even if the voltage of the switch line SR is set at 0.7 V and the current I1 flowing in the MOSFETs m7 and m8 is made lower when the control line CTRL is at 0 V, the ferromagnetic tunnel junction element MTJ1 switches from a low resistance to a high resistance as long as the absolute value of the current I1 is greater than Ic. Even if the voltage of the switch line SR is set at 0.7 V and the absolute value of the current 12 flowing in the MOSFETs m7 and m8 is made lower when a positive voltage is applied to the control line CTRL, the ferromagnetic tunnel junction element MTJ2 switches from a high resistance to a low resistance as long as the absolute value of 12 is greater than the absolute value of Ic. Furthermore, even if the voltage of the control line CTRL is set at 0.4 V, the ferromagnetic tunnel junction element MTJ2 switches from a high resistance to a low resistance. As described above, the voltages of the switch line SR and the control line CTRL are made lower, so that power consumption can be lowered, and storing can be performed.

[0052] The absolute value of the current 12 is greater than that of the current I1, because the source of the MOSFET m7 is connected to the control line CTRL via a resistor (a ferromagnetic tunnel junction element) while the source of the MOSFET m8 is connected to the node QB.

[0053] FIGs. 12A and 12B are diagrams each illustrating simulations performed to simulate characteristics of the bistable circuit during the store period. FIGs. 12A and 12B show the voltage of the node QB relative to the node Q when current is flowing in the ferromagnetic tunnel junction elements during the store period. The arrows indicate the scanning directions in the simulations. In FIG. 12A, the dotted lines, the dashed lines, and the solid lines indicate cases where the voltage of the switch line SR is 1.1 V, 0.85 V, and 0.7 V, respectively, when the ferromagnetic tunnel junction element MTJ1 is switched from a low resistance to a high resistance (or when the control line is at 0 V in FIG. 11). As shown in FIG. 12A, as the voltage of the switch line SR becomes lower, the noise margin of the bistable circuit 30 becomes wider.

[0054] In FIG. 12B, the solid lines, the dashed line, and the dotted lines indicate cases where the voltages of the switch line SR and the control line CTRL are 1.1 V and 0.65 V, 0.85 V and 0.5 V, and 0.7 V and 0.4 V, respectively, when the ferromagnetic tunnel junction element MTJ2 is switched from a high resistance to a low resistance (or when the control line is at a positive voltage in FIG. 11). As shown in FIG. 12B, as the voltages of the switch line SR and the control line CTRL become lower, the noise margin of the bistable circuit 30 becomes wider.

[Third Embodiment]

[0055] The structure of a memory circuit of a third embodiment is the same as that of the first embodiment illustrated in FIGs. 5A and 5B, and therefore, explanation thereof is not repeated herein. FIG. 13 is a timing chart illustrating

simulations performed to simulate the supply voltage Vsupply and the voltage of the switch line SR during the restore period, and the currents I1 and I2 flowing in the ferromagnetic tunnel junction elements MTJ1 and MTJ2 during the restore period. The simulations were performed in cases where the ferromagnetic tunnel junction element MTJ1 had a high resistance, and the ferromagnetic tunnel junction element MTJ2 had a low resistance. The dotted lines indicate a case where the voltage of the switch line SR was 1.1 V (VDD), and the solid lines indicate a case where the voltage of the switch line SR was 0.7 V. When the supply voltage Vsupply is rising, the solid line indicates a lower value than the dotted line in each of the cases with the currents I1 and 12. Accordingly, power consumption can be lowered.

[0056] FIGs. 14A through 14C are diagrams each illustrating simulations performed to simulate changes in potential at the nodes Q and QB during the restore period. In the diagrams, the ferromagnetic tunnel junction elements MTJ1 and MTJ2 have a high resistance and a low resistance, respectively, and the voltage of the switch line SR is 1.1 V, 0.85 V, and 0.7 V. FIGs. 14A through 14C correspond to cases where the increase rate of the supply voltage when the supply voltage Vsupply during the restore period is ramped up is 0.011 V/n sec, 0.11 V/n sec, and 1.1 V/n sec, respectively. At any of the increase rates, when the voltage of the switch line SR is 0.7 V, the voltage of the node QB does not become higher, and the voltage VQ of the node Q is restored at a high level. As described above, data is restored into the bistable circuit 30 in a more stable manner when the voltage of the switch line SR is low.

[0057] According to the second and third embodiments, the control unit 85 performs control so that the voltage to be applied to the gates of the MOSFETs m7 and m8 during the period to store data written in the bistable circuit 30 into a nonvolatile element in a nonvolatile manner (the store period) or during the period to restore data stored in a nonvolatile element in a nonvolatile manner into the bistable circuit 30 (the restore period) becomes lower than the supply voltage Vsupply to be applied to the bistable circuit 30 during the period to write data into and read data from the bistable circuit 30 in a volatile manner (the normal period). In this manner, power consumption can be lowered, and the bistable circuit 30 can be maintained in a stable state. Further, the bistable circuit 30 can also be maintained in a stable state by increasing the rate at which the supply voltage increases.

[0058] As in the third embodiment, the control unit 85 performs control so that the highest voltage to be applied to the control line CTRL during the store period becomes lower than the supply voltage Vsupply. In this manner, power consumption can be lowered, and the bistable circuit 30 can be maintained in a stable state.

[0059] Although preferred embodiments of the present invention have been described so far, the present invention is not limited to those particular embodiments, and various changes and modifications may be made to them within the scope of the invention clamed herein.

DESCRIPTION OF REFERENCE NUMERALS

[0060]

10, 20	inverter
30	bistable circuit
85	control unit
MTJ1, MTJ2	ferromagnetic tunnel junction element

Claims

1. A memory circuit comprising:

a bistable circuit (30) configured to write data;
a nonvolatile element (MTJ1, MTJ2) configured to store data written in the bistable circuit (30) in a nonvolatile manner by changing a resistance value with a current flowing between one end and the other end and restore data stored in a nonvolatile manner into the bistable circuit (30), the nonvolatile element (MTJ1, MTJ2) having the one end connected to a node (Q, QB) in the bistable circuit (30) and the other end connected to a control line (CTRL);
an FET (m7, m8) having a source and a drain connected in series to the nonvolatile element (MTJ1, MTJ2) between the node (Q, QB) and the control line (CTRL); and **characterized in that** the memory circuit further comprises:
a control unit (85) configured to make a highest voltage (SR) to be applied to a gate of the FET (m7, m8) during a period to restore data stored in the nonvolatile element (MTJ1, MTJ2) in a nonvolatile manner into the bistable circuit (30) lower than a voltage of a node being at a high level in the bistable circuit (30) during a period to write data into and read data from the bistable circuit (30) in a volatile manner.

2. The memory circuit according to claim 1, wherein the control unit (85) is further configured to make the highest voltage (SR) to be applied to the gate during a period to store data written in the bistable circuit (30) into the nonvolatile element (MTJ1,MTJ2) in a nonvolatile manner lower than the voltage of the node being at a high level in the bistable circuit (30) during the period to write data into and read data from the bistable circuit (30) in a volatile manner.

3. The memory circuit according to claim 1 or 2, wherein the control unit (85) is further configured to make the highest voltage to be applied to the control line (CTRL) during a period to store data written in the bistable circuit (30) into the nonvolatile element (MTJ1, MTJ2) in a nonvolatile manner lower than the voltage of the node being at a high level in the bistable circuit (30) during the period to write data into and read data from the bistable circuit (30) in a volatile manner.

Patentansprüche

1. Speicherschaltung, welche aufweist:

eine bistabile Schaltung (30), die zum Schreiben von Daten konfiguriert ist;
ein nicht-flüchtiges Element (MTJ1, MTJ2), das konfiguriert ist, um in die bistabile Schaltung (30) geschriebene Daten durch Ändern eines Widerstandswerts mit einem zwischen einem Ende und dem anderen Ende fließenden Strom in nicht-flüchtiger Weise zu speichern, und in nicht-flüchtiger Weise gespeicherte Daten in die bistabile Schaltung (30) zurückzuspeichern, wobei das eine Ende des nicht-flüchtigen Elements (MTJ1, MTJ2) mit einem Knoten (Q, QB) in der bistabilen Schaltung (30) verbunden ist und sein anderes Ende mit einer Steuerleitung (CTRL) verbunden ist;
einen FET (m7, m8), dessen Source und Drain in Serie mit dem nicht-flüchtigen Element (MTJ1, MTJ2) zwischen dem Knoten (Q, QB) und der Steuerleitung (CTRL) verbunden sind; und
dadurch gekennzeichnet, dass die Speicherschaltung ferner aufweist:
eine Steuereinheit (85), die konfiguriert ist, um eine höchste Spannung (SR), die an ein Gate des FET (m7, m8) anzulegen ist, während einer Zeitdauer, um in dem nicht-flüchtigen Element (MTJ1, MTJ2) in nicht-flüchtiger Weise gespeicherte Daten in die bistabile Schaltung (30) zurückzuspeichern, niedriger zu machen als eine Spannung eines Knotens, die in der bistabilen Schaltung (30) während einer Zeitdauer, um in flüchtiger Weise Daten in die bistabile Schaltung (30) zu schreiben und Daten aus dieser zu lesen, auf einem hohen Pegel ist.

2. Die Speicherschaltung nach Anspruch 1, wobei die Steuereinheit (85) ferner konfiguriert ist, um die höchste Spannung (SR), die an das Gate anzulegen ist, während einer Zeitdauer, um in die bistabile Schaltung (30) geschriebene Daten in das nicht-flüchtige Element (MTJ1, MTJ2) in nicht-flüchtiger Weise zu speichern, niedriger zu machen als die Spannung des Knotens, die in der bistabilen Schaltung (30) während der Zeitdauer, um in flüchtiger Weise Daten in die bistabile Schaltung (30) zu schreiben und Daten aus dieser zu lesen, auf einem hohen Pegel ist.

3. Die Speicherschaltung nach Anspruch 1 oder 2, wobei die Steuereinheit (85) ferner konfiguriert ist, um die höchste Spannung, die an die Steuerleitung (CTRL) anzulegen ist, während einer Zeitdauer, um in die bistabile Schaltung (30) geschriebene Daten in das nicht-flüchtige Element (MTJ1, MTJ2) in nicht-flüchtiger Weise zu speichern, niedriger zu machen als die Spannung des Knotens, die in der bistabilen Schaltung (30) während der Zeitdauer, um in flüchtiger Weise in die bistabile Schaltung (30) zu schreiben und Daten aus dieser zu lesen, auf einem hohen Pegel ist.

Revendications

1. Circuit de mémoire comprenant :

un circuit bistable (30) configuré pour écrire des données ;
un élément non volatil (MTJ1, MTJ2) configuré pour stocker des données écrites dans le circuit bistable (30) d'une manière non volatile en changeant une valeur de résistance par un courant s'écoulant entre une extrémité et l'autre extrémité et pour restaurer des données stockées d'une manière non volatile dans le circuit bistable (30), l'élément non volatil (MTJ1, MTJ2) ayant l'une extrémité connectée à un nœud (Q, QB) dans le circuit bistable (30) et l'autre extrémité connectée à une ligne de commande (CTRL) ;
un FET (m7, m8) ayant une source et un drain connectés en série à l'élément non volatil (MTJ1, MTJ2) entre le nœud (Q, QB) et la ligne de commande (CTRL) ; et
caractérisé en ce que le circuit de mémoire comprend en outre :

une unité de commande (85) configurée pour rendre une tension la plus haute (SR) à appliquer à une grille du FET (m7, m8) pendant une période pour restaurer des données stockées dans l'élément non volatil (MTJ1, MTJ2) d'une manière non volatile dans le circuit bistable (30) inférieure à une tension d'un nœud étant à un haut niveau dans le circuit bistable (30) pendant une période pour écrire des données dans le circuit bistable (30) et lire des données de celui-ci d'une manière volatile.

2. Circuit de mémoire selon la revendication 1, dans lequel l'unité de commande (85) est en outre configurée pour rendre la tension la plus haute (SR) à appliquer à la grille pendant une période pour stocker des données écrites dans le circuit bistable (30) dans l'élément non volatil (MTJ1, MTJ2) d'une manière non volatile inférieure à la tension du nœud étant à un haut niveau dans le circuit bistable (30) pendant la période pour écrire des données dans le circuit bistable (30) et lire des données de celui-ci d'une manière volatile.

3. Circuit de mémoire selon la revendication 1 ou 2, dans lequel l'unité de commande (85) est en outre configurée pour rendre la tension la plus haute à appliquer à la ligne de commande (CTRL) pendant une période pour stocker des données écrites dans le circuit bistable (30) dans l'élément non volatil (MTJ1, MTJ2) d'une manière non volatile inférieure à la tension du nœud étant à un haut niveau dans le circuit bistable (30) pendant la période pour écrire des données dans le circuit bistable (30) et lire des données de celui-ci d'une manière volatile.

FIG. 1A

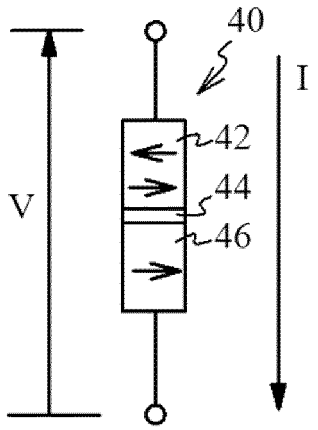


FIG. 1B

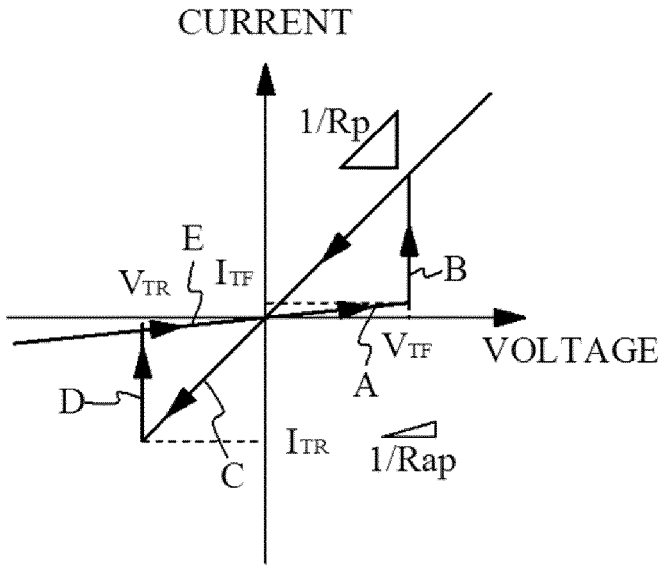


FIG. 1C

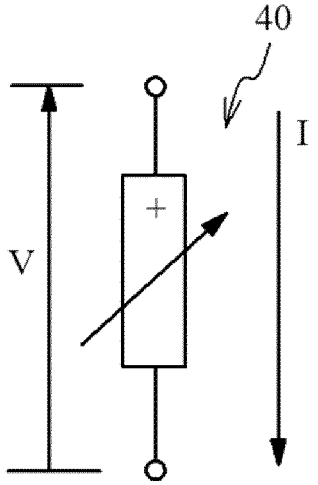


FIG. 2

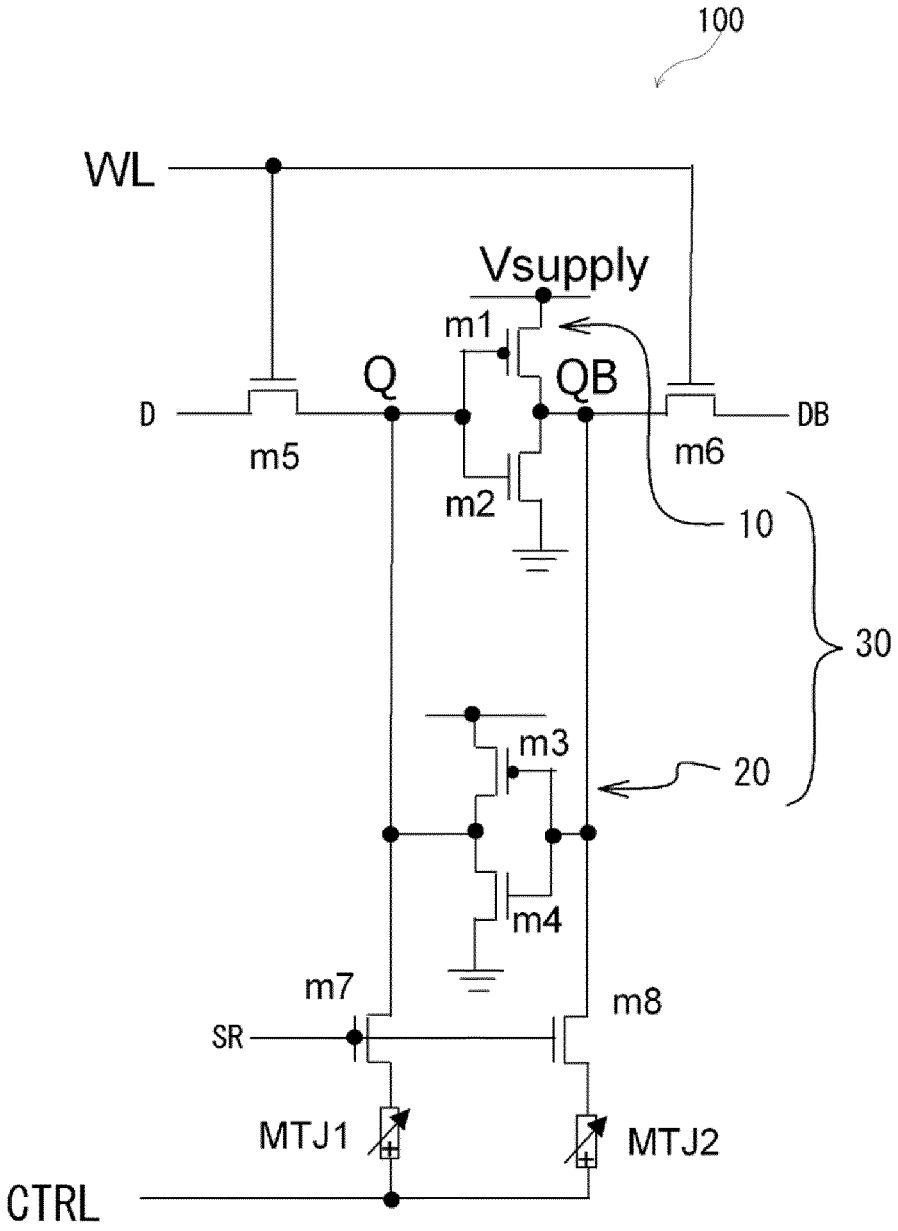

100
WL
Vsupply
m1
Q
QB
D
DB
m5
m6
m2
10
30
m3
20
m4
m7
m8
SR
MTJ1
MTJ2
CTRL

FIG. 3

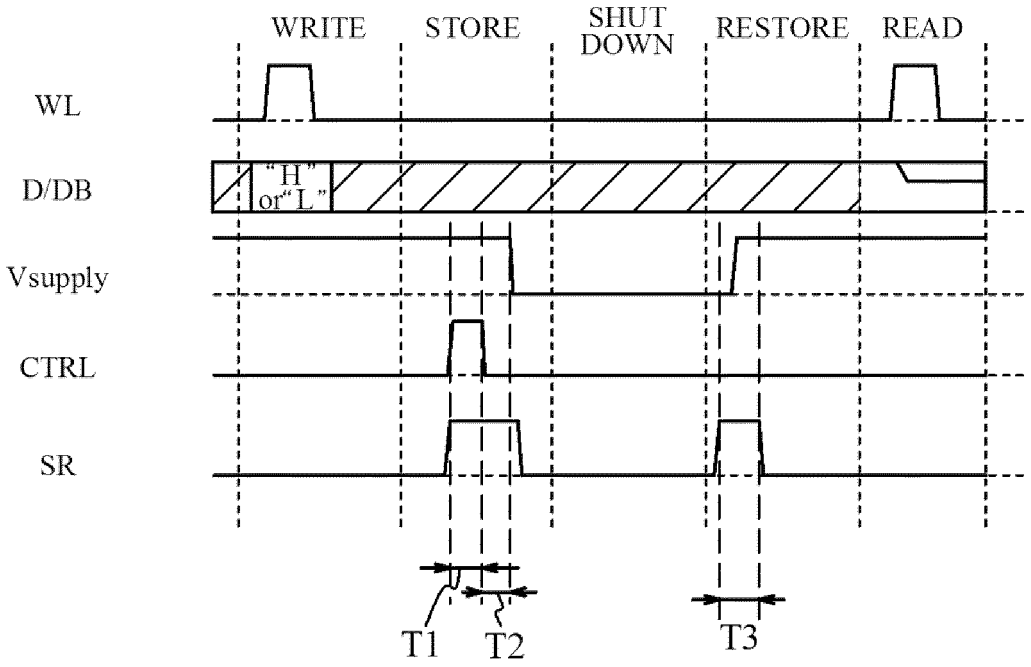

WRITE
STORE
SHUT DOWN
RESTORE
READ
WL
D/DB
"H" or "L"
Vsupply
CTRL
SR
T1
T2
T3

FIG. 4A

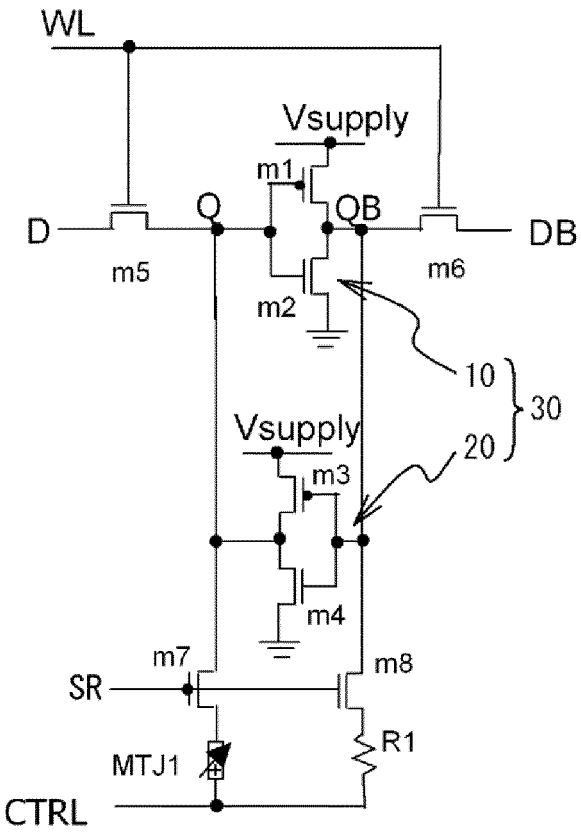

WL
Vsupply
m1
D
Q
QB
DB
m5
m6
m2
10
30
Vsupply
20
m3
m4
m7
m8
SR
R1
MTJ1
CTRL

FIG. 4B

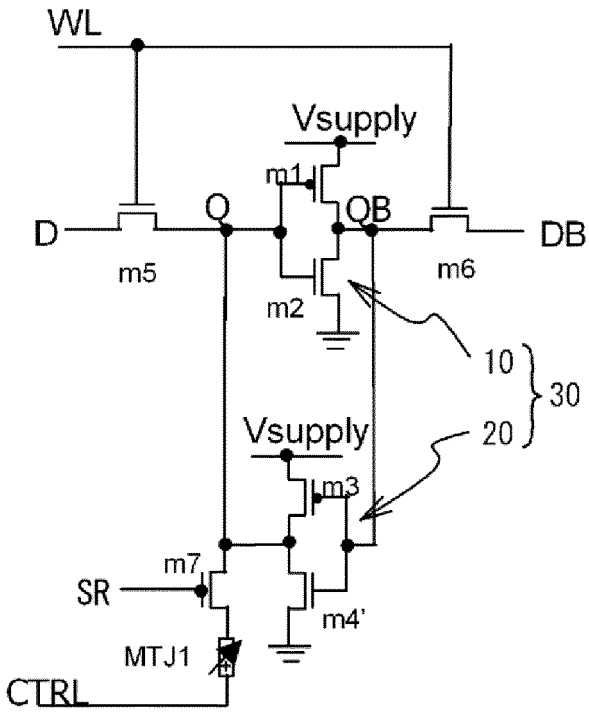

WL
Vsupply
m1
D
Q
QB
DB
m5
m6
m2
10
30
Vsupply
20
m3
m7
SR
m4'
MTJ1
CTRL

FIG. 5A

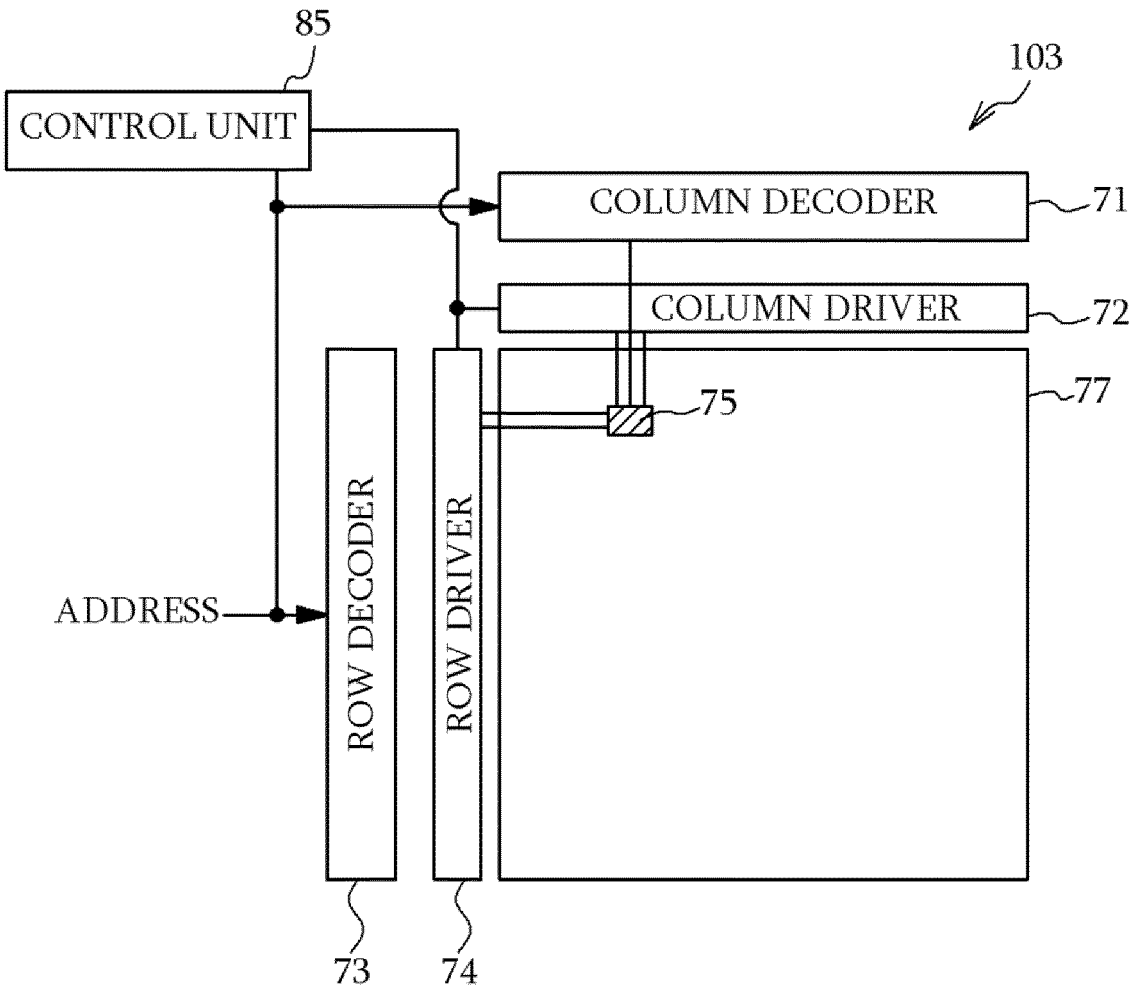

85
CONTROL UNIT
103
COLUMN DECODER
71
COLUMN DRIVER
72
75
77
ADDRESS
ROW DECODER
ROW DRIVER
73
74

FIG. 5B

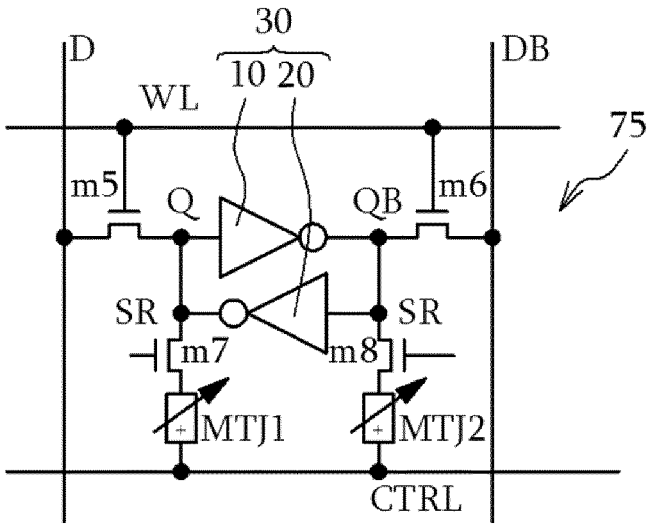

D
30
10 20
DB
WL
75
m5
Q
QB
m6
SR
SR
m7
m8
MTJ1
MTJ2
CTRL

FIG. 6

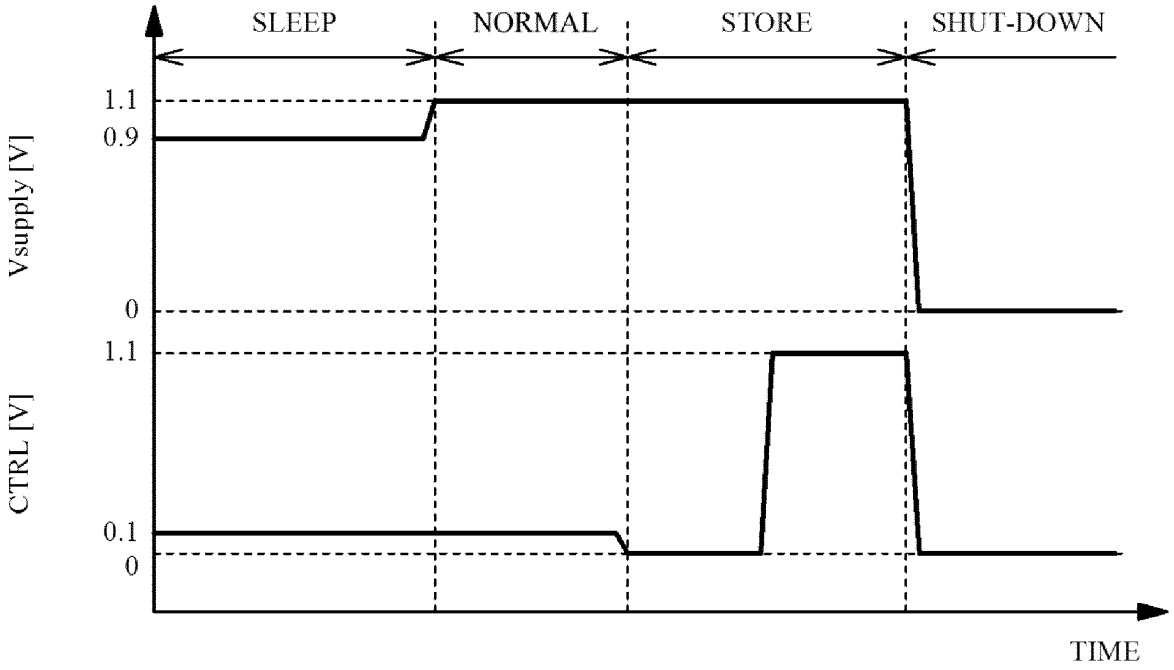

SLEEP
NORMAL
STORE
SHUT-DOWN
1.1
0.9
Vsupply [V]
0
1.1
CTRL [V]
0.1
0
TIME

FIG. 7

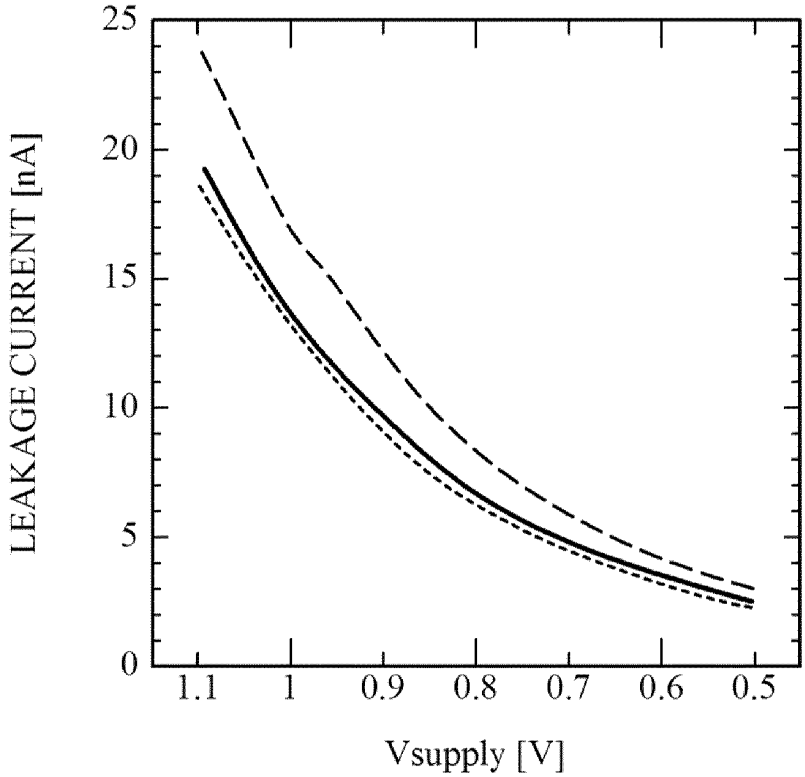

25
20
15
10
5
0
LEAKAGE CURRENT [nA]
1.1
1
0.9
0.8
0.7
0.6
0.5
Vsupply [V]

FIG. 8

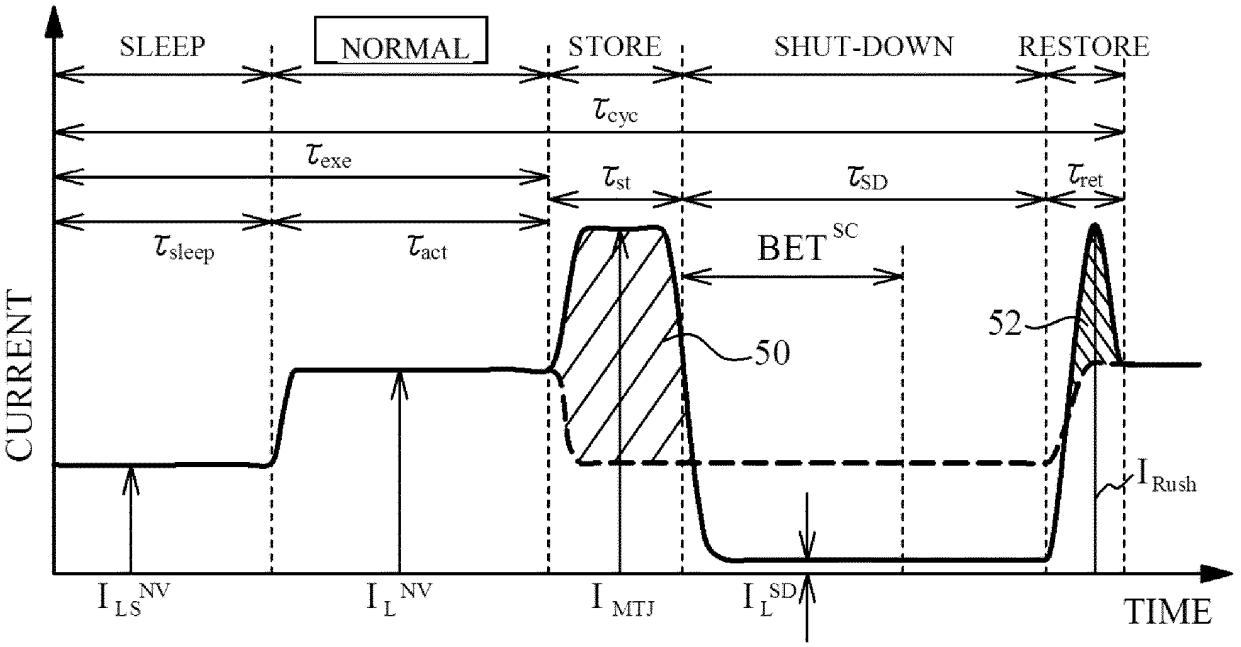

SLEEP
NORMAL
STORE
SHUT-DOWN
RESTORE
τ_{cyc}
τ_{exe}
τ_{st}
τ_{SD}
τ_{ret}
τ_{sleep}
τ_{act}
BET SC
50
52
CURRENT
I_{Rush}
I_{LS}^{NV}
I_{L}^{NV}
I_{MTJ}
I_{L}^{SD}
TIME

FIG. 9

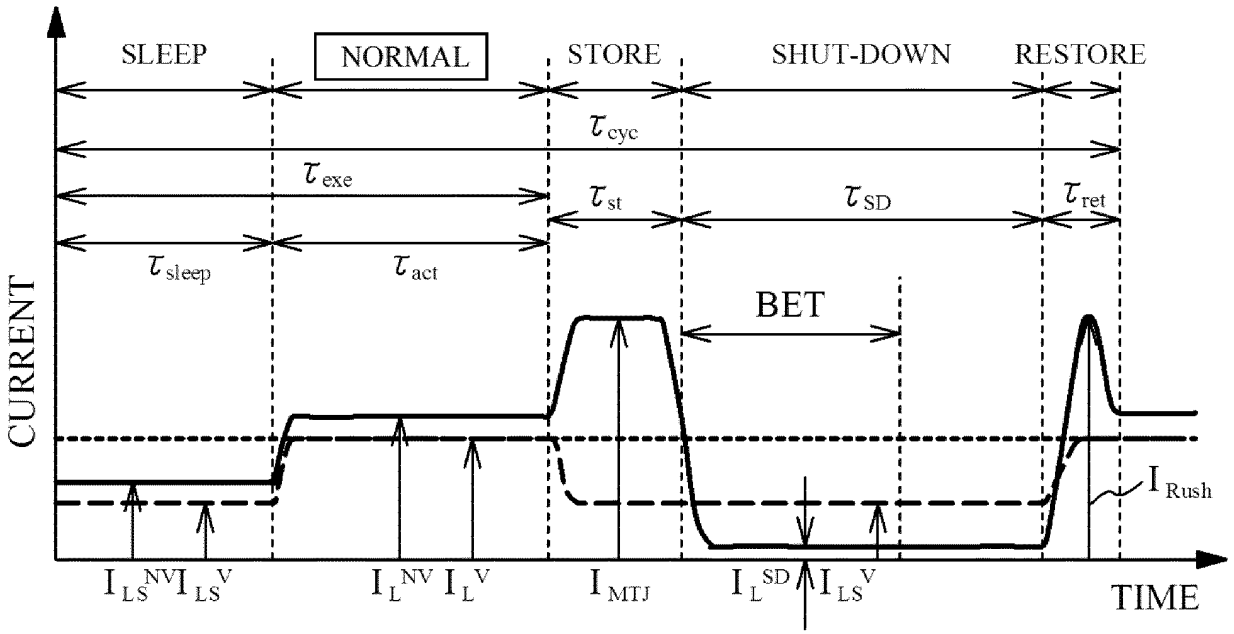

SLEEP
NORMAL
STORE
SHUT-DOWN
RESTORE
τ_{cyc}
τ_{exe}
τ_{st}
τ_{SD}
τ_{ret}
τ_{sleep}
τ_{act}
BET
CURRENT
I_{Rush}
I_{LS}^{NV} I_{LS}^{V}
I_{L}^{NV} I_{L}^{V}
I_{MTJ}
I_{L}^{SD} I_{LS}^{V}
TIME

FIG. 10

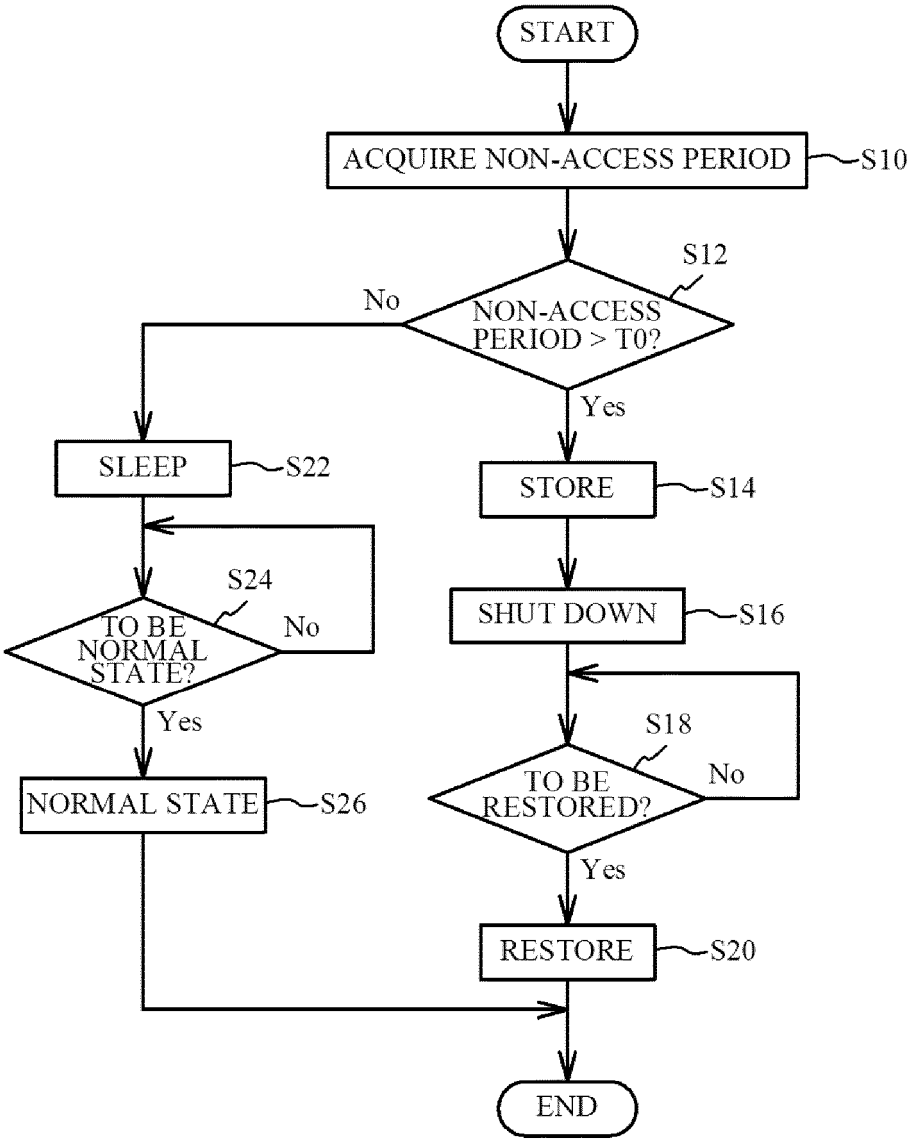

START
ACQUIRE NON-ACCESS PERIOD
S10
S12
NON-ACCESS PERIOD > T0?
No
Yes
SLEEP
S22
STORE
S14
S24
TO BE NORMAL STATE?
No
SHUT DOWN
S16
Yes
S18
TO BE RESTORED?
No
NORMAL STATE
S26
Yes
RESTORE
S20
END

FIG. 11

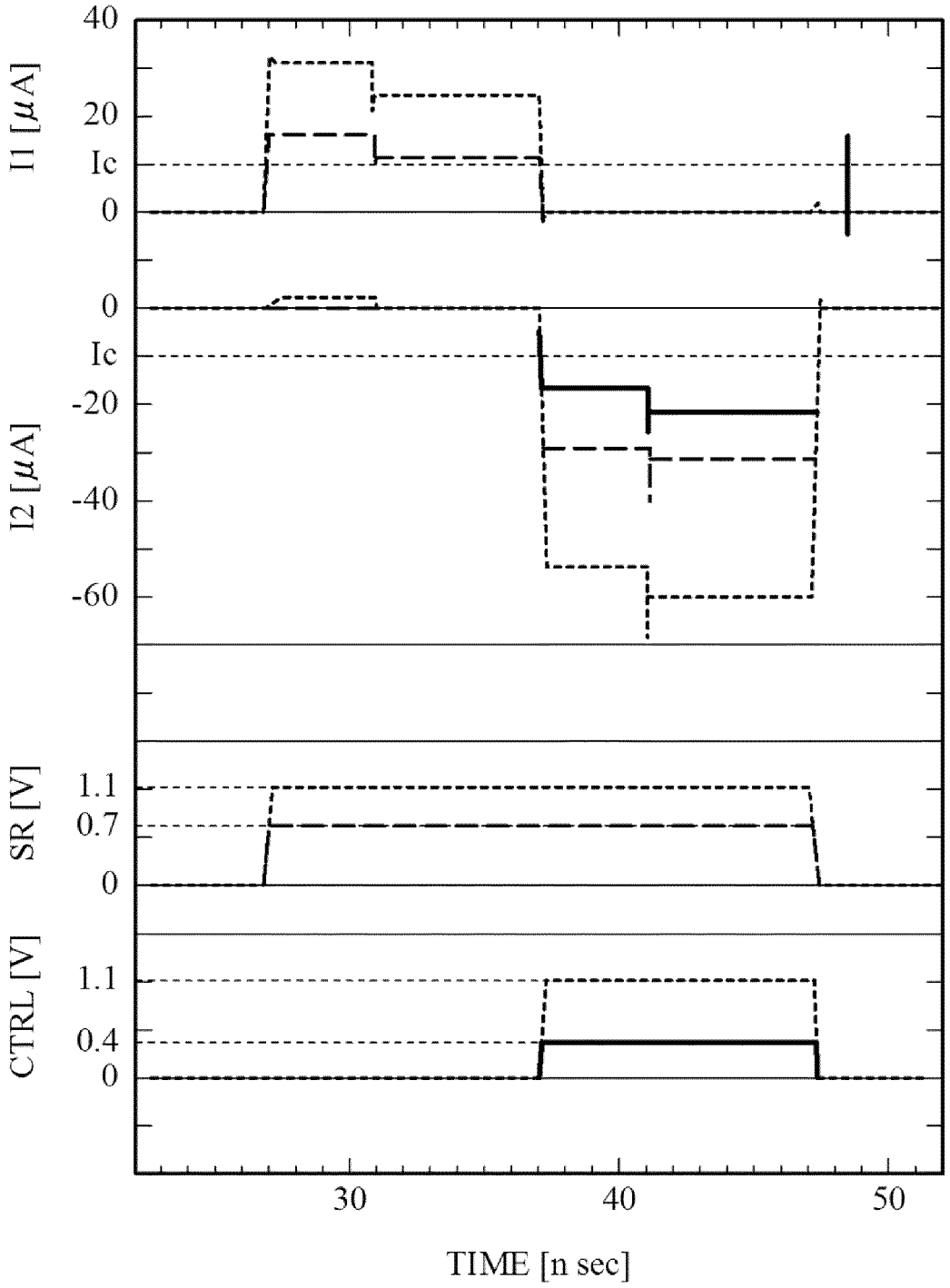

40
20
Ic
0
I1 [μA]
0
Ic
-20
-40
-60
I2 [μA]
1.1
0.7
0
SR [V]
1.1
0.4
0
CTRL [V]
30
40
50
TIME [n sec]

FIG. 12A

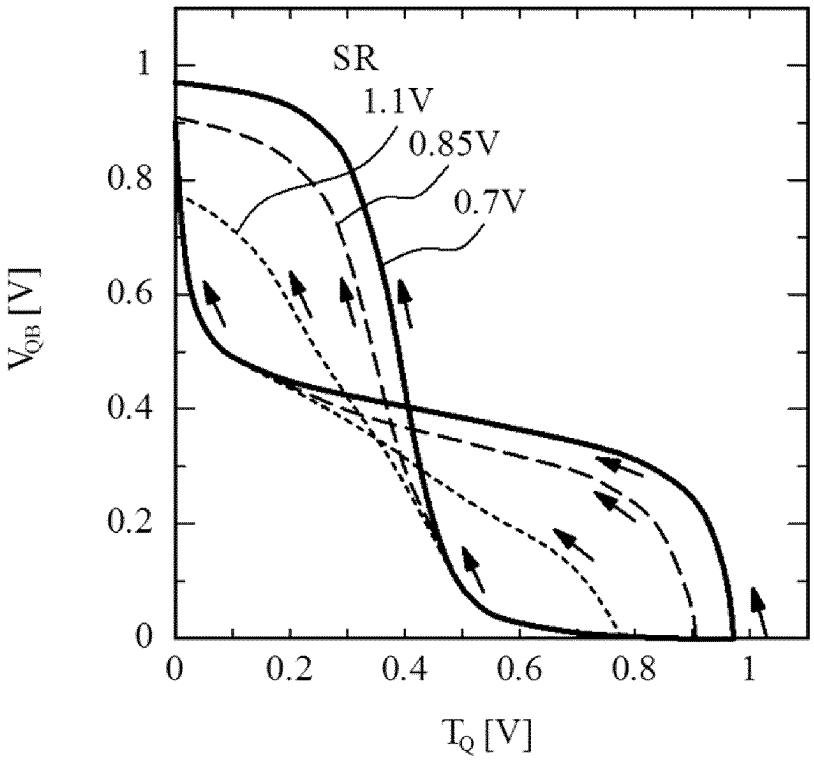


FIG. 12B

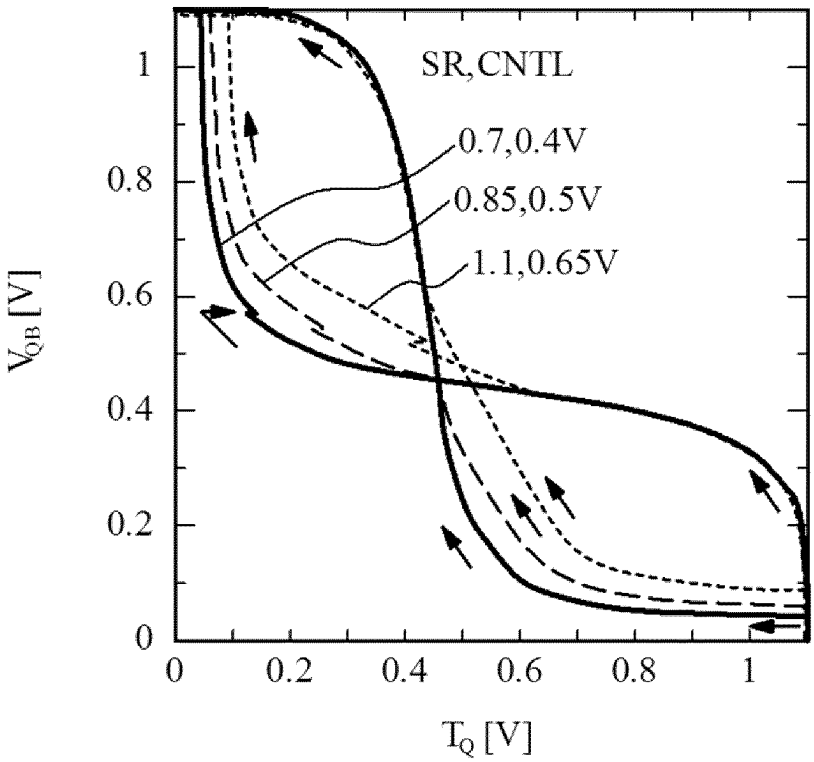


FIG. 13

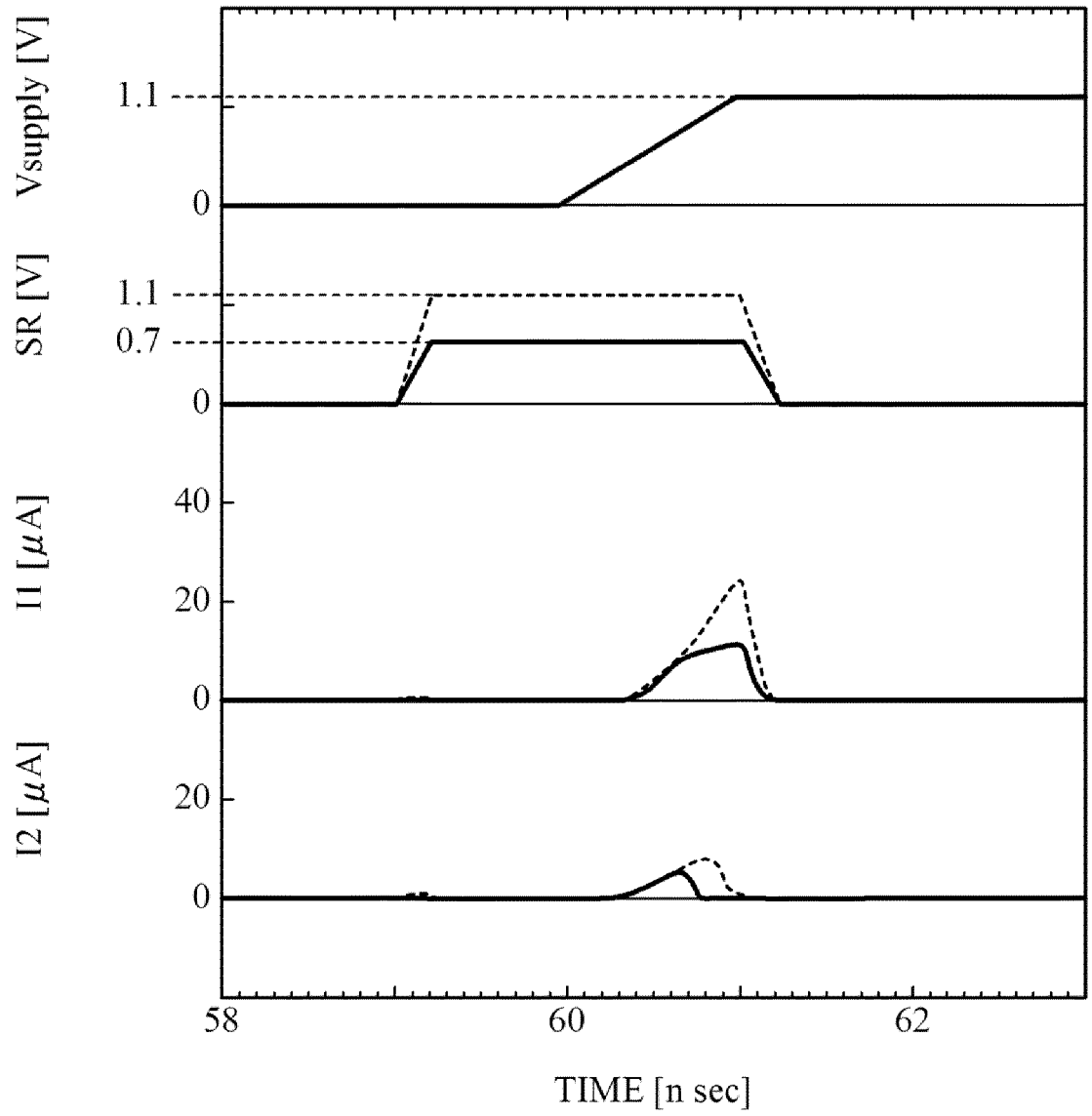


FIG. 14A

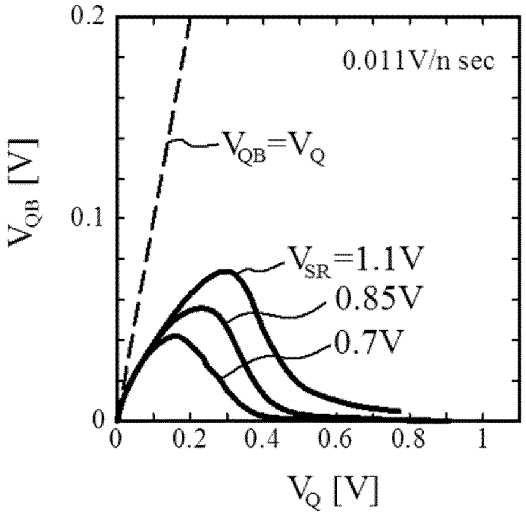


FIG. 14B

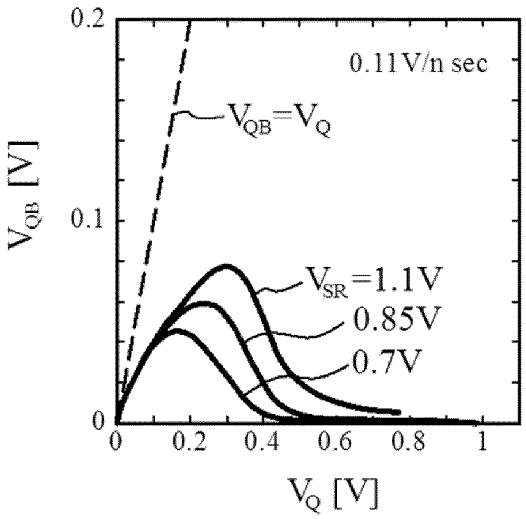
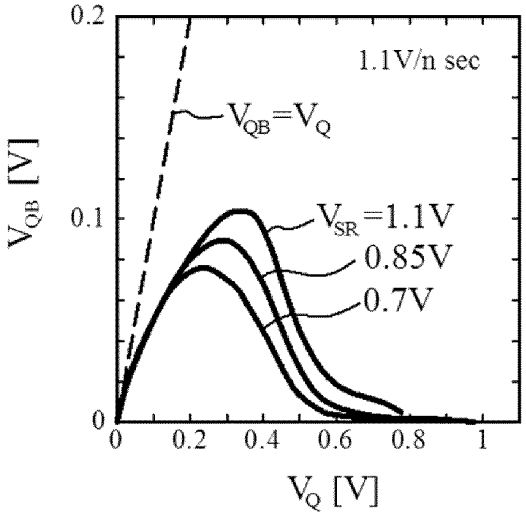


FIG. 14C



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 2009028298 A **[0004]**

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