System Integration of Quantum-Scale Devices

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Introduction

With the progress of computer technology, the problems related to the ultimate performance of the computer are being discussed from various points of view, *e.g.*, how to cope with the exponential explosion of the amount of computation, how to sense the outer world and make soft and instantaneous decisions like a human brain, and how should we carry out the hardware down-scaling facing to the area of atomic dimensions. In this project, we are investigating the solution for these problems within a framework of silicon technology and its extension, utilizing both quantum effects in nanoscale structure and quantum-analogous phenomena with ordinary devices, adopting the approaches some of which from the basic device physics upward and some from the system architecture downward, to construct novel concepts of the computing system. For these purposes we are doing researches in four groups, the profiles and activities of which are to be introduced in the following. Details will appear on the abstract by each group in the following pages and on the posters during this symposium.

Hardware Realization of Quantum-Comparable Computational Ability in Silicon[1)]

This group is supervised by the author together with Dr. M. Fujishima. The purpose of this group is to develop a novel computing system which can alleviate the exponentially exploding complexity of computation to be confined within a polynomial increase of computational time and hardware. Our choice is to make a challenge to this by using silicon technologies and its extension, expecting to realize the machine within a future reachable for us.

For the first step, we have made an experiment of hardware emulation of quantum computing by using the integrated circuits, the finite impulse response (FIR) filters.[1)2)] In quantum computing, the logic states are expressed by n qubits which are the superposition of basis vectors ortho-normalized in $2^n(=N)$-dimensional space. We map these basis to discrete N slots in the frequency domain and represent the logic signal $x(k)$ in the form of a Fourier series in $\exp(j2\pi ak/N)$, a = 0,1,2,----,N-1, with the coefficients $X(a)$ determined by DFT(Discrete Fourier Transform) of $x(k)$, where the time k is made discrete with the time interval Δ.

As an actual hardware demonstration, we have fabricated an experimental system which performs Grover's algorithm for the database search by using FPGAs (Field-Programmable Gate Arrays) as shown in Fig. 1. In our experiment, the 3-qubit case that gives $N = 2^3 = 8$ was performed.

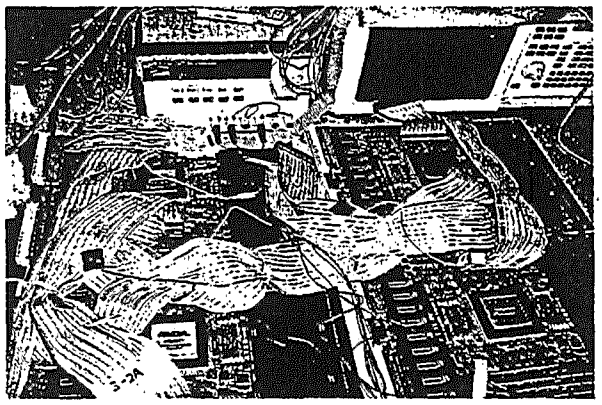

Fig. 1. An emulation engine for quantum computer implemented in FPGAs *Altera EPF10K250A*

Grover's elementary operations consist of three kinds of unitary matrices. The Walsh-Hadamard transform W, the conditional phase inversion C (N-dimensional) in which only diagonal elements are non-zero and all unity but for the state($k = k_0$) to be chosen as the answer, *i.e.*, c (k_0,k_0) = –1, and another N-dimensional phase inversion P with only diagonal elements being non-zero and all unity except for p (0,0) = –1.

Starting from the initial eigenstate $|X_{init}> = [1\ 0\ 0\ 0\ 0\ 0\ 0\ 0]^t$, a serial combination of unitary transformations ($-WPWC$) is operated twice. Twice is sufficient because theoretically this needs be operated for the times not exceeding $N^{1/2}$. The resultant final state is obtained as $|X_{fin.}> = [-1\ -1\ -1\ \mathbf{11}\ -1\ -1\ -1\ -1]^t / 128^{1/2}$. The power spectra of the experimental results are shown in Fig.2 for the states k = 0 to 7. Small probabilities of appearance

scatter on the states besides the correct answer, $k = k_0 = 3$, depending on the processing accuracy in the experiment.

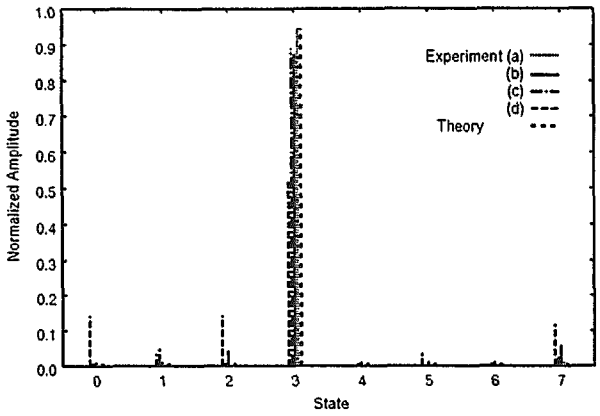

Fig.2 Power spectra of the results of Grover's algorithm. Experimental parameters for the level spacing Δ, internally processed bit number and the rounding-off scheme are, (a) $\Delta = 2^{-7}$, 10bits, half-adjusting, (b) $\Delta = 2^{-7}$, 7bits, half-adjusting, (c) $\Delta = 2^{-7}$, 7bits, trancating and (d) $\Delta = 2^{-6}$, 6bits, trancating, respectively.

Our system is free from decoherence with which many proposals for genuine quantum computer are haunted. On the other hand, the present method cannot by itself cope with the exponential increase of computational time and hardware. Based on the knowledge we have get from this emulation, we are seeking the way to deal with these problems to realize the practically feasible computing system whose performance is close to those expected from quantum computing, whether the physical principle we will adopt may be identical or not.

Resonant-type Intelligent Agent[3]

This group is supervised by Professor T. Shibata. He has developed the ν(neuron)-MOS transistor circuits which has been utilized for universal logic functions in integrated circuits and, above all, for intelligent functions such as pattern recognition (see, for example, Ref.4)). His work has been extended[5][6] in the present project to the development of more sharply tuned image recognition system by utilizing a resonantly tuned characteristics either of a quantum effect device such as the resonant-tunneling MOSFET, another invention by Professor Shibata, or of the silicon circuits which show Λ-shaped I-V characteristics equivalent to the resonant response. To realize the latter, a novel CMOS circuit shown in Fig.3 has been developed and designed. With this circuit, the sharpness of the resonance can be freely changed as shown in Fig.4.

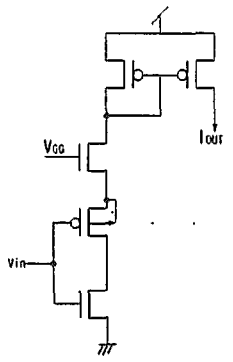

Fig. 3 CMOS resonant agent circuit.

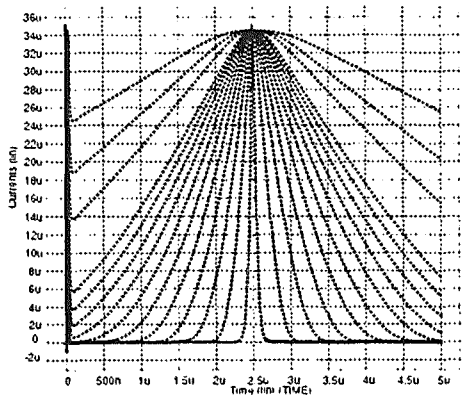

Fig. 4 Resonant response of the circuit in Fig.3. The input voltage is ramped from 0 volt to V_{DD} within 6 μs.

The pattern recognition circuit based on the novel feature extraction algorithm for the visual image has been developed with successful results.[6] This is the method that extracts the characteristic vector from the image by enhancing the edges, not only those parallel to the vertical and horizontal axes, but additionally to the axes rotated by $\pm 45^\circ$. The effectiveness of this circuit has been demonstrated, for example, in the automatic identification of the landmark in cephalometry in which some characteristic points should be identified on the x-ray photographs of the patient's scull for the purpose of dental care. It was assured by the collaborating M.D. that the system developed by Shibata group is more skillful than most of the young dentists under training in identifying these characteristic points. Therefore this can be the first step to the realization of the soft computer with the ability of human sense and decision.

Clustered Electron Memory Using Silicon Quantum Dots[7]

This group, supervised by Dr. T. Hiramoto, has been very actively carrying out the study of single-electron devices on the basis of silicon technology and has realized one of the best and clearest characteristics of the single-electron devices at temperatures up to the room temperature (see, for example, Ref.8)). In the present project, his work has been extended to the utilization of larger number of electrons (some tens to hundreds). This number is much larger than that used in single electron devices but still far below the number used in the present VLSI memory, tens of thousands electrons. Thus the operation with the reliability much higher than the single electron memory and yet with the power dissipation much lower than VLSI memory can be expected. For this purpose, the size and the spatial distribution of quantum dots must be controlled accurately.[7] This group has fabricated such type of device with the combination of a single-electron transistor (SET) and the multi-dot memory[9] as illustrated in Fig.5, containing the silicon dots with the diameter 8nm prepared by CVD. A poly-silicon control gate is placed over the device.

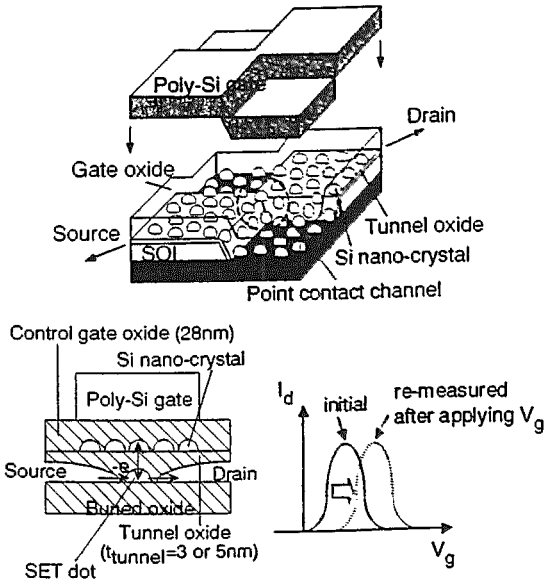

Fig. 5 Controllable single-electron device with quantum dots.

With this device, they succeeded in the external precise control of the device characteristics[10] as shown in Fig.5. It can be seen in this figure that the *I-V* curve of the device can be shifted to the non-overlapping position by applying the control-gate voltage. Such complete separation is favorable for the digital inverter operation of this device. This control method has been further extended to the separate control of two devices integrated as shown in Fig.6. *I-V* curves of two SETs are separately controlled by the control-gate voltage as shown in Fig. 7 and this lead to the realization of the directional current switch.[11]

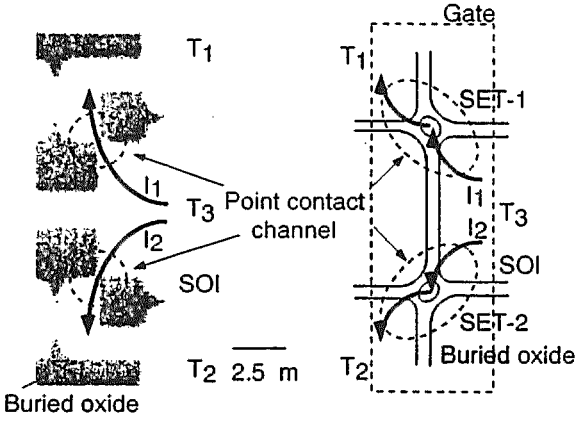

Fig. 6 Integrated single-electron devices.

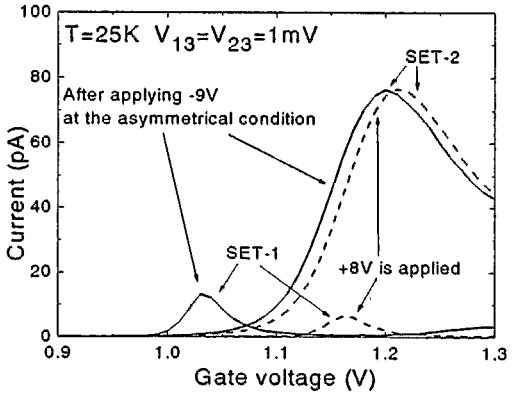

Fig. 7 Characteristics control of the integrated single-electron devices in Fig.6.

Air-Bridge Silicon Nanowire[12]

Supervised by Dr. J. Itoh, this group has long been evaluated highly for their development of nano-scale vacuum microelectronic devices such as cold electron emitters by an exquisite process technologies (see, for example, Ref.13)). Extending these technologies, in the present project they experimentally fabricated aerial (air-bridge) nanowires of silicon and are evaluating their characteristics.[14] The nanowire they have fabricated has typically the cross section of 20nm

×40 nm as shown in Fig.8. Its *I-V* curve shows Λ-shape as shown in Fig.9 which is attributed to the effects of the slow surface states on the wire covered by the native oxide.[15] The effect has the dependence on the ambient pressure and shows hysteresis.[12] To clarify the cause of these phenomena, the electric field distribution in the device was measured with the scanning Maxwell-stress microscope (SMM) before and after the occurrence of the hysteresis. It was found that the potential distribution along the wire became inhomogeneous after the hysteresis occurred.[12] This inhomogeneity may hinder the current to flow in the wire in the same manner as it was in the initial state.

Because this wire is air-bridged, there are several possibilities to make 3-dimensional novel structure for functional devices which can be utilized by other groups in our team. Presently they are fabricating a dual-gate MOS transistor which preliminary shows the function similar to MNOS memory.[12]

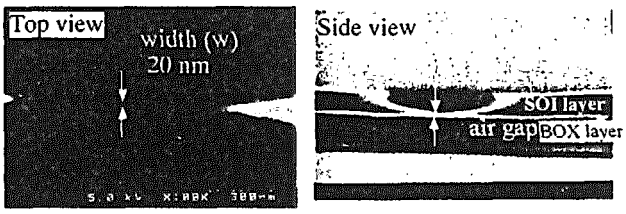

Fig. 8 Air-bridge silicon nanowire.

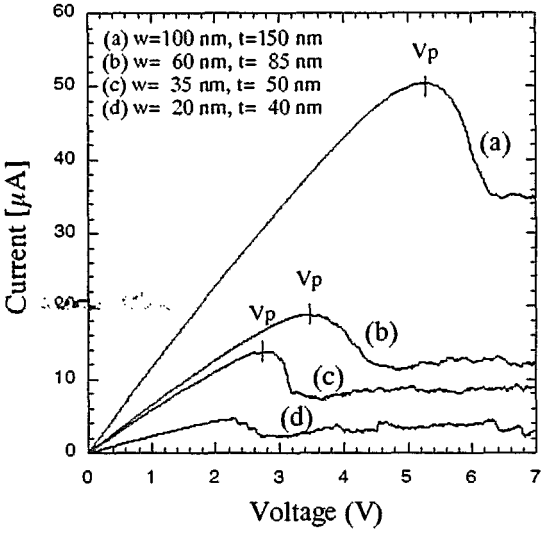

Fig. 9 *I-V* characteristics of air-bridge nanowires.

Concluding Remarks

The present status of the activities of our research team has been reviewed. On the basis of these achievements, we are further pushing the way to make them utilize for each other to realize novel types of basic elements of computing system such as processors, agents, memories, *etc.* and to construct the concepts of the powerful and soft computing system.

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