Hardware Emulation of Quantum Computing:
Towards the Realization of Quantum-Comparable Computational Ability on Silicon

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Quantum computing is expected to realize massive parallel computation by using delicate quantum physics. To attain improved computational ability in the near future, however, we should better construct a system by using practically available silicon technology. Therefore, we are trying to map mathematical nature of quantum computing into VLSI. For the first step, we have designed a hardware emulation engine for the quantum computing with the integrated FIR (Finite Impulse Response) filters [1]. Our hardware emulates the evolution of wave functions by the unitary transformation operated upon the oscillatory signals which represents a superposed state.

In quantum computing, the logic states are expressed by n qubits which are the superposition of basis vectors ortho-normalized in $2^n(=N)$-dimensional space. We map these basis to discrete N slots in frequency domain and represent the logic signal $x(k)$ in the form of a Fourier series in $\exp(j2\pi ak/N), a = 0, 1, 2, \ldots, N-1$, with the coefficients $X(a)$ determined by DFT (Discrete Fourier Transform) of $x(k)$, where the time k is made discrete as $k = t/\Delta$ with the time interval Δ. In our emulator, the unitary transformation of logic states is realized by performing the transformation on the N-dimensional state vector $|X\rangle$ whose components are $X(a)$'s. As is shown in Fig. 1, an $N \times N$ unitary transformation matrix U is realized by utilizing N parallel complex FIR filters combined with N cyclic frequency shift units denoted by "**C**". The unit **C** circulates $X(a)$ by multiplying a time-dependent signal $\exp(j2\pi k/N)$. By this circuit, oscillatory signals which represent the initial state $|X\rangle$ are transformed to the appropriate signals which represent the final state $|Y\rangle$.

We performed an experimental verification of this emulation engine by using field-programmable gate-arrays (FPGAs). Grover's algorithm for database searching [2] was chosen as an example. This algorithm has a merit of requiring only $O(N^{1/2})$ attempts for searching N elements. In our experiment, the 3-qubit case that gives $N = 2^3 = 8$ was performed. The oscillatory signals were represented by digitally-alternating waveforms and digital FIR filters were implemented in the FPGA *Altera EPF10K250A* with the maximum operating frequency of 5 MHz. As the initial state $|X_{\text{init}}\rangle = [1\ 0\ 0\ 0\ 0\ 0\ 0\ 0]$, a constant pattern of amplitude 0.125 was fed into the input node. The state was then evolved so as to emphasize the logic state which was to be chosen as searching subjective, and the oscillatory pattern appeared at the output as shown in Fig. 2 (a). This time-dependent signal was transformed by DFT to the frequency spectra which correspond to $|X_{\text{fin}}\rangle$. Figure 2 (b) shows their power spectra which represent the appearance probability of the states $k = 0$ to 7. The spectral strength of the state corresponding to the correct answer, $k = 3$ in this case, is observed the highest. Theoretically, this should be higher than other states by a factor 121.

Based on the knowledge about the evolution of the states in the computation, we are seeking the way to realize the computing system whose performance is close to those expected from quantum computing.

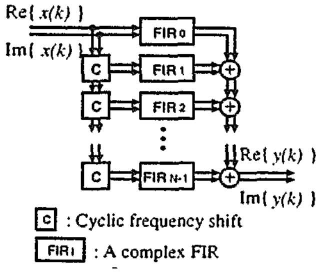

Fig. 1. A circuit configuration of the unitary transformation U.

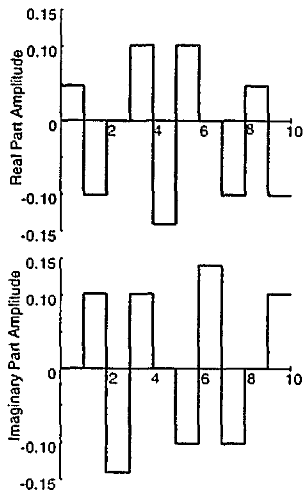

Fig. 2. The waveform appeared at output node in the time domain. Quantization level spacing: 2^{-7}. Internal process: 10 bits. Rounding off scheme: half-adjusting.

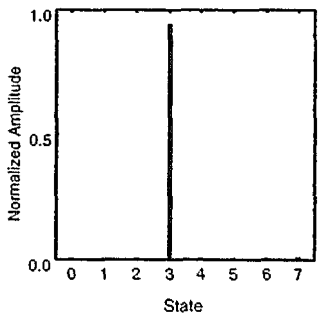

Fig. 3. The normalized power spectra of the output as shown in Fig. 2.

References

[1] S. O'uchi, M. Fujishima and K. Hoh: *Extended Abstract of the 1999 Int. Conf. on Solid State and Materials* (The Japan Society of Applied Physics, Tokyo, 1999) p. 96.

[2] L. K. Grover: Phys. Rev. Lett. **79**, (1997) 325.