Mesoscopic Properties of Silicon Quantum Dots

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Motivation for Ballistic Transport: Ballistic transport effect is promising for future electron devices featuring no fluctuation and higher conduction, compared to conventional silicon devices. However, ballistic transport in silicon has been observed only when the sample is cooled in dilution refrigerator or by AC measurement using lock-in technique because of a short mean free path. Here, we report clear quantized conductance in Si measured at 3K by DC mode using a vertical transistor. In a vertical transistor, the channel length is defined by a thickness of a gate electrode, 25nm, deposited by CVD. The channel width can be controlled by electric field confinement, using a wrap gate. Poly-Si channel, prepared by solid phase crystallization (SPC) of CVD a-Si, is very high quality with a grain size of 200nm and a mean free path of 40nm. Measurement under magnetic field allows discussion of the transport mechanism. The vertical transistor was fabricated on a substrate consist of SiO_2(30nm)/poly-Si(25nm)/SiO_2(30nm)/Si. Poly-Si as a gate electrode was fabricated by CVD and SPC of a-Si. By EB lithography, a 60nm×60nm square was patterned. Two SiO_2 layers were etched anisotropically by ECR-RIE. Poly-Si layer was etched isotropically by plasma etching. Then, as a gate oxide, TEOS SiO_2 thickness 20nm was deposited, followed by annealing. The TEOS SiO_2 layer was etched by ECR-RIE. Then poly-Si by SPC of a-Si by CVD, with $10^{18}/cm^3$ phosphorus doping, was deposited. The grain size of larger than 200nm guarantees that the device channel is free of a grain boundary, which limits the electron mean free path.

Characteristics and Discussions: The current path is controlled by depleting the channel caused by applied gate voltage. At a low bias voltage of 1mV and temperature of 3K, conductance changed as staircase-like characteristics. The staircase shape was broadened as the temperature was increased. This characteristic was expected in a ballistic transport. Because of the unique sample geometry, the channel size can be much smaller than the electron mean free path. Moreover, by depleting the channel, the distance between the channel and the SiO_2 interface increases, so the scattering at the interface is decreased. Because of heavily doped channel, electric field in the depleted region is high, so a confinement effect of the channel is strong. It prevents carriers from scattering between subbands. Moreover, the conductance in ballistic region was five times higher than that in no ballistic region with a high bias voltage. Under magnetic field, a unit of quantized conductance was divided by two or four. This means that degeneracy of spin and valley was split.

Another Application of Ballistic Transport: A Cold Electron Emitter using Nanocrystalline Silicon Ballistic transport effect enables another application such as a cold electron emitter. A planer type electron emitter with narrow beam dispersion formed by porous Si (PS) has also been proposed to improve the electron efficiency, the difficulty of fabrication processes, and other problems in conventional planer type electron emitter. The authors suggest the dominant mechanism is that hot electrons ballistically transported through the PS layer. An external quantum efficiency of about 1% defined by the ratio of the emission current to the total current was achieved. In this case, a wet etching process was used and it is hard to control the size of the nanocrystal (nc) dots in PS. This makes both investigating mechanism and improving the device performance difficult. Direct deposition of uniform nc-Si material is expected to be a promising candidate of fabricating high efficiency electron emitters. The nc-Si thin films have been fabricated by using VHF plasma CVD with well-controled crystal sizes. A high emission ratio comparable to PS was obtained and more device optimization experiments are in progress. An n^+-Si (0.01Ωcm) wafer was used as the substrate and the electron source. The Si nanodots with diameters of about 10±5 nm have been deposited on the substrate at room temperature by plasma CVD. The CVD system includes a plasma cell, which is separated from UHV chamber by a stainless steel plate with an orifice. Ar and SiH_4 gases, whose flow rates were 10sccm and 1sccm, respectively, exited by 144MHz plasma with a power of 3W. The Si nanodots were formed in the gas phase by coalescence of SiH_4 radicals and extracted out of the plasma cell through the orifice to the Si wafer. The thickness of the nc-Si layer was 600nm. Afterwards, the samples were oxidized at 700°C for 1hour and then 1000°C for 5minutes for covering the dots with SiO_2 and for forming a thin oxide layer in the surface. Finally, an Ohmic electrode in the backside of Si and a 10nm-thick Au film in the surface were formed.

Characteristics and Discussions: Measurements were performed in vacuum with a base pressure of 10^{-6}torr. The Au electrode was grounded, and a metal plate as a collector of electrons extracted into a vacuum was located above the sample by the distance of 5mm and applied a constant positive voltage of 100V. While a negative voltage was applied to the Si substrate, a simple diode current was observed. When a negative voltage over 5V was applied, which related to the work function of Au on Si, electrons started to be extracted from the sample and reached to the collector. At a voltage of −36V, an emission efficiency of over 0.8% was obtained. The device structure allows a clear understanding of the mechanism for electron emission. A possible process proposed for PS emitter is as follows; First electrons are injected from a silicon wafer into nc-Si dots without scattering due to small size of dots. The electric field is applied mainly within SiO_2 regions covering the dots. Thus the electrons from nc-Si are therefore accelerated in SiO_2 by the high electric field, allowing ballistic transport through subsequent nc-Si layers. Since there is high controllability of nc-Si size, further detailed investigations of mechanism can be performed, which will lead to the improvement of the device performance.

Conclusion: We presented two devices taking advantage of ballistic transport effect. One application is the vertical structure device. This device with a small dimension enable to observe clear conductance quantization resulting from ballistic transport. We confirmed the increased current drivability due to ballistic transport. We also fabricated cold electron emitter using nc-Si. An emission efficiency of 0.8% was obtained. High controllability of nc-Si dots enables detailed investigations, leading to high electron efficiency.