Single Electron Memory Devices based on Nanocrystalline Silicon Quantum Dots

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A promising approach for high density/low power consumption memory devices is to store a single charge in a nano-scale memory node, which affects electron transport in a nearby channel. In order to study the mechanism of charge retention, a flexible design that is sensitive to the charge of a single dot is required. Our approach to make the active region of the device sensitive to a single charged dot is to simply define by e-beam lithography a narrow channel (40nm length by 30nm width) on thin (20nm) Silicon-on-Insulator (SOI). Onto this nc-Si are deposited by a high-throughput gas phase nucleation and growth process using pulsed-source remote plasma enhanced CVD, which forms 6±2nm diameter nc-Si dots. This process affords a well-defined storage node with low interfacial defect density. Room temperature threshold hysterisis from a single electron stored in nc-Si dot results in a threshold shift of 90 mV, which is expected for a 8nm diameter nc-Si dot over a 30nm wide channel as calculated by Coulombic shift of channel surface potential. Importantly discrete stepwise increase in channel current is seen for single electron emission process that can be analyzed as a function as time in a statistical manner. Lifetimes are seen to show a Poisson's distribution; that is the standard deviation is nearly equal to the mean, which is expected for a process with high attempt frequency and low probability of success. Analysis of memory lifetime as a function of temperature shows a $1/T^2$ dependence, which is characteristic of a direct tunneling process. Thus interfacial defect states with dot (which would show thermal activation trend) can be eliminated and not influence memory retention time. Figure 1 shows the modeling of lifetime as a function of gate bias, accounting for electron distribution within dot. A classical approach to electron distribution within the dot is used due to long lifetime compared to electron wave function coherence time. Nc-Si dot size is seen to be an important parameter in isolating charge away from channel, thus enabling an increase in retention time.

To control location of nc-Si, a new selective chemical surface treatment is proposed. Selectivity is based on the attraction between carboxylic and amine functional groups. Such selectivity has been demonstrated for nc-Au/SiO_2 systems, however a new synthetic scheme is applied to nc-Si/SiO_2 system. An advantage of this scheme is that e-beam or AFM lithography can pattern the monolayers thus the controlling spatial location of where nc-Si are deposited. Importantly, organic monolayers are readily removed by oxidation to form defect free Si/ SiO_2 tunnel barriers.

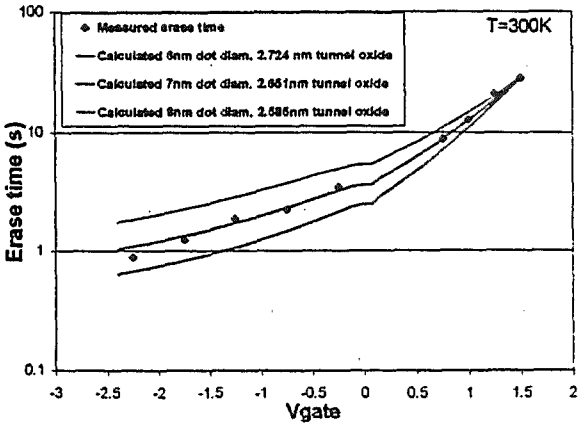

Figure 1. Measured and calculated memory retention time as a function of gate bias. Modeling is based on direct tunneling process accounting for electron distribution in dot. Tunnel rate is normalized at Vg=1.5V by tunnel barrier thickness.

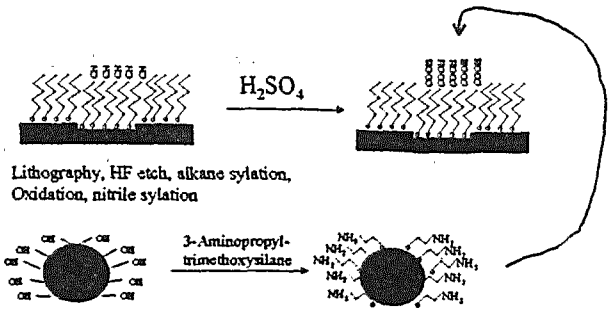

Figure 2. Synthetic scheme for chemical alignment of nc-Si dots onto lithographically defined areas of chemical selectivity. Patterned areas of substrate can be directly defined by e-beam lithography or AFM patterning. Alternately, of opposite functionality can be assembled to form well defined multiplayer structure.