Few-electron transport properties of Si and poly-Si nanostructures

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Silicon and polycrystalline silicon (poly-Si) based nanostructures have been widely used as a key building block for Coulomb blockade memory and logic devices. In these structures nanometer-scale electron islands naturally formed by random dopant distribution and/or grain boundaries (GBs) are utilised to achieve the Coulomb blockade characteristics. However, microscopic aspects of these naturally-formed islands and the details of electron tunnelling in these structures have not been fully understood. This paper presents recent experimental and theoretical study of the mechanism of few-electron transport in Si and poly-Si nanowires.

For investigating discrete aspects of the GBs, we have fabricated nano-butterfly (NB) poly-Si transistor structures (Fig. 1) which enable us to characterize single or a few GBs in a ultra-short channel. First, an amorphous-Si film with a thickness of 50 nm was deposited on 40-nm-thick SiO_2, followed by phousphorous ion implantation (20keV 5×10^{14} cm^{-2}). Then, solid phase crystallization was performed by annealing at 850°C for 30 minutes. The average grain size was estimated to be approximately 20 nm by SEM and TEM observation. The NB channel structures were defined by e-beam lithography and electrically isolated by reactive ion etching. Temperature dependence of the I-V characteristics were measured for the NB transistors with channel width and length as small as 30nm. Figure 2(a) shows typical non-linear Ids-Vds characteristics which are attributable to single or a few GBs in the NB channel. From the temperature dependence of the resistivity in the high temperature region (Fig. 2(b)), a potential barrier height V_B of the GBs was evaluated from 10 to 77 meV. Various values of V_B obtained for the NB devices are supposed to show different local potential minima along the GB potential barrier for conducting electrons.

For investigating the effects of random dopant distribution in silicon nanowires, we have developed a simulator which includes the random dopants in the device explicitly. We make the approximation that the electron distribution is two dimensional and calculated self-consistently in the potential landscape of the dopants under the Thomas-Fermi approximation at T=0 K. The islands of electrons produced by this procedure are then assumed to have sufficiently metallic-like properties that we can calculate inter-island capacitances. We make the extremely crude assumption that the tunnel resistance between islands scales exponentially with shortest distance between the islands and use the resulting information to form a netlist as an input into a single-electron simulator. For sufficiently low biases, we make a reasonable assumption that the island sizes don't change significantly and hence neither does the capacitance or tunnel resistance. Thus we are able to simulate the IV characteristics of a nanowire as the gate voltage is changed. Our initial studies are aimed at examining the statistics of the threshold voltage and the effects of random offset charges. Figure 3 shows the unbiased electron distribution in a nanowire and the resultant IV characteristic, the gate voltage is relative to the gate voltage resulting from asserting the particular Fermi level to get the islands shown.

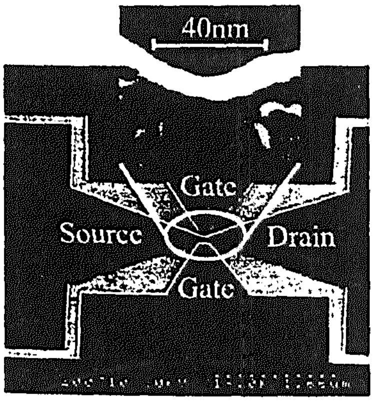

Figure 1: Top down SEM images of nano-butterfly poly-Si transistor.

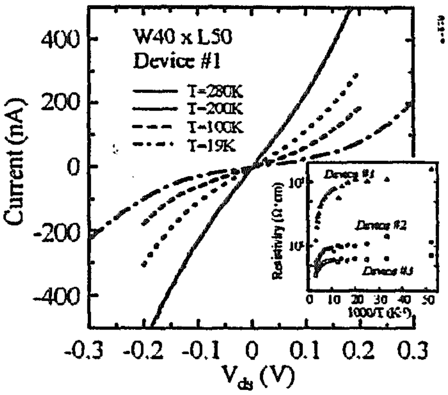

Figure 2: I_{ds}-V_{ds} characteristics and temperature dependence (the inset) of resistivity for the poly-Si nanostructure devices.

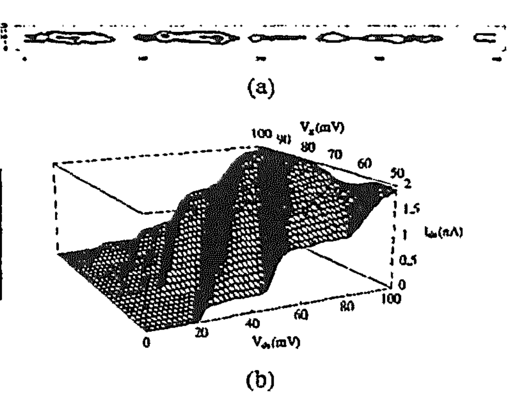

Figure 3: a) shows islands of electrons trapped in minima of the dopant potential landscape and b) shows the I_{ds}-V_{ds}-V_g characteristic for biases close to those that produced (a).

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